



MS-7295 Ver:1.1

CPU:

AMD 940 Athlon 64/Athlon 64 FX

System Chipset:

NVIDIA C51PV / C51PVG

NVIDIA MCP 51

On Board Chipset:

LPC Super I/O -- Winbond 83627EHF

LAN REALTEK RTL8211BL

HD Codec --ALC883

BIOS --LPC FLASH ROM 4M

Main Memory:

DDR * 4 (Max 4GB)

Expansion Slots:

PCI-E X 16 *1

PCI-E X 4 *1

PCI 2.3 Slot * 2

PWM:

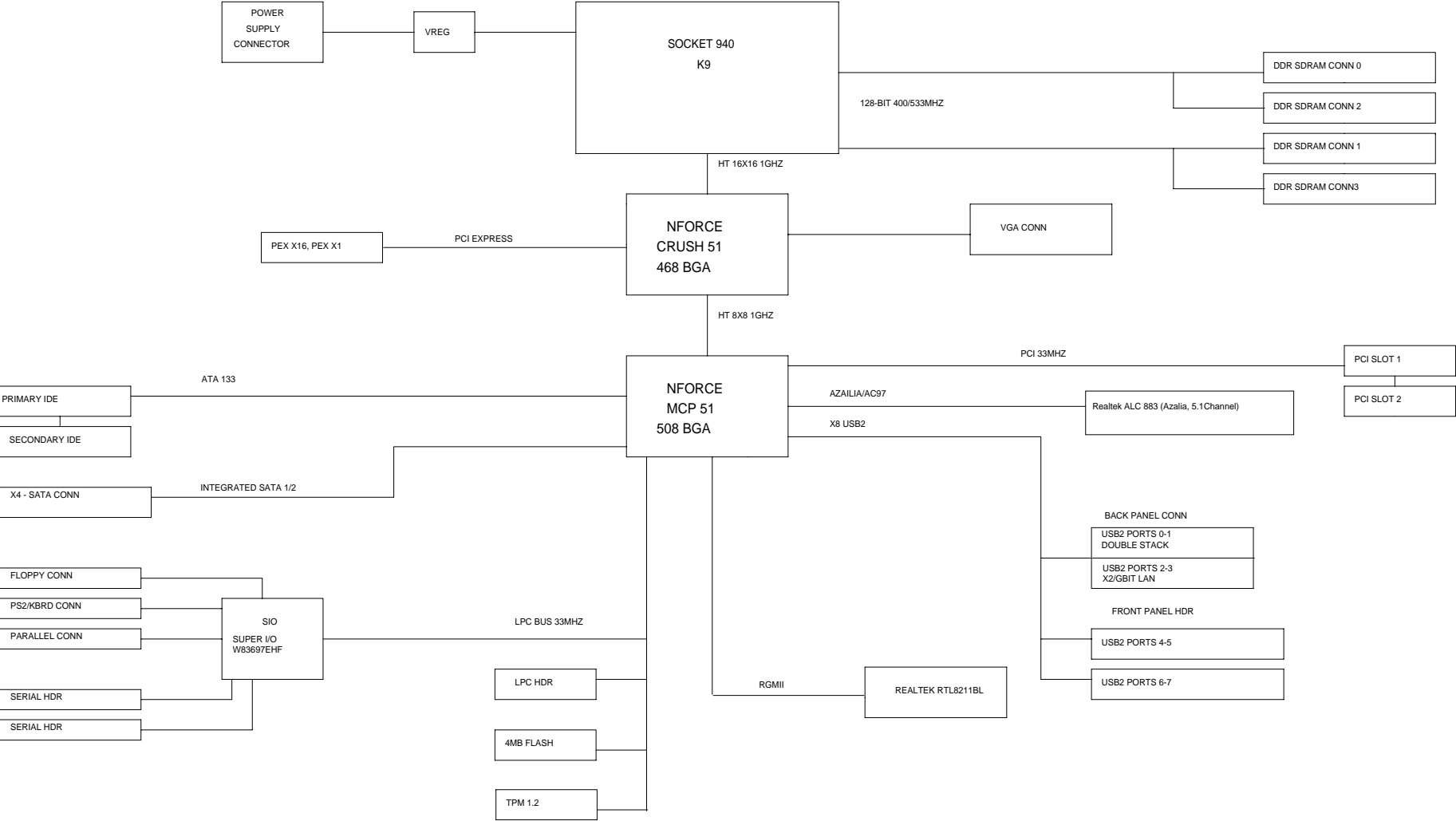
Controller--Intersil ISL6566CR 3 Phase

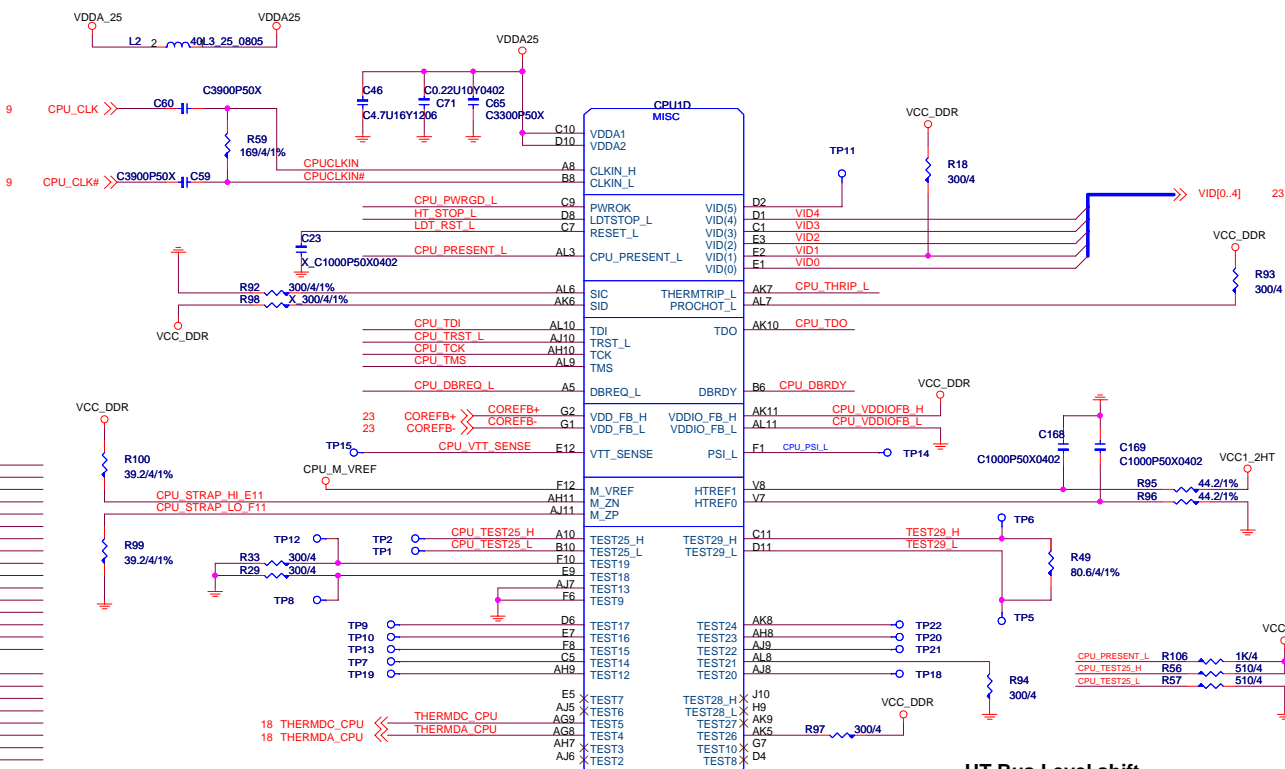
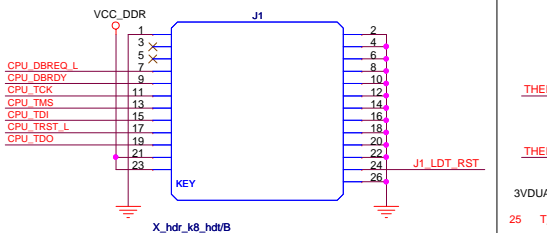
Title	Page
Cover Sheet	1
Block Diagram	2
AMD M2 940	3,4,5
System Memory	6,7
DDR Terminations	8
C51PVG	9-11
MCP51	12-15
PCI Slot 1,2	16
PCI-Express X 16 , X4 Slot	17
SIO-Winbond83627EHF / BIOS	18
LAN - REALTEK RTL8211BL	19
Azalia CODEC ALC883 & Interanl SPK	20
USB connectors	21
MS-6 ACPI Controller & MS-6+	22
PWM - ISL6566CRZ	23
IDE &FDD & FAN	24
ATX Connector / Front Panel	25
VGA Connector	26
DVI CONNECTOR	27
COM PORTS & TPM1.2	28
TEST POINTS & PCB	29
History	30-31
GPIO SPEC	32
POWER OK MAP	33
POWER MAP	34
MANUAL PARTS	35

NECCI BOGOTA

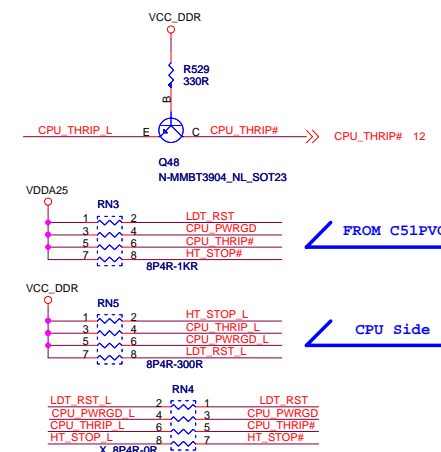
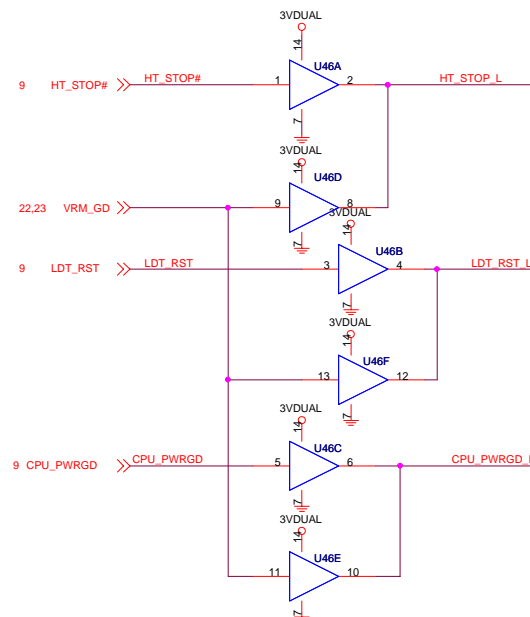
Micro Star Restricted Secret		
Title	Cover Sheet	Rev 1.1
Document Number	MS-7295	
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St., Jung-Hsi City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Wednesday, August 01, 2007 Sheet 1 of 35

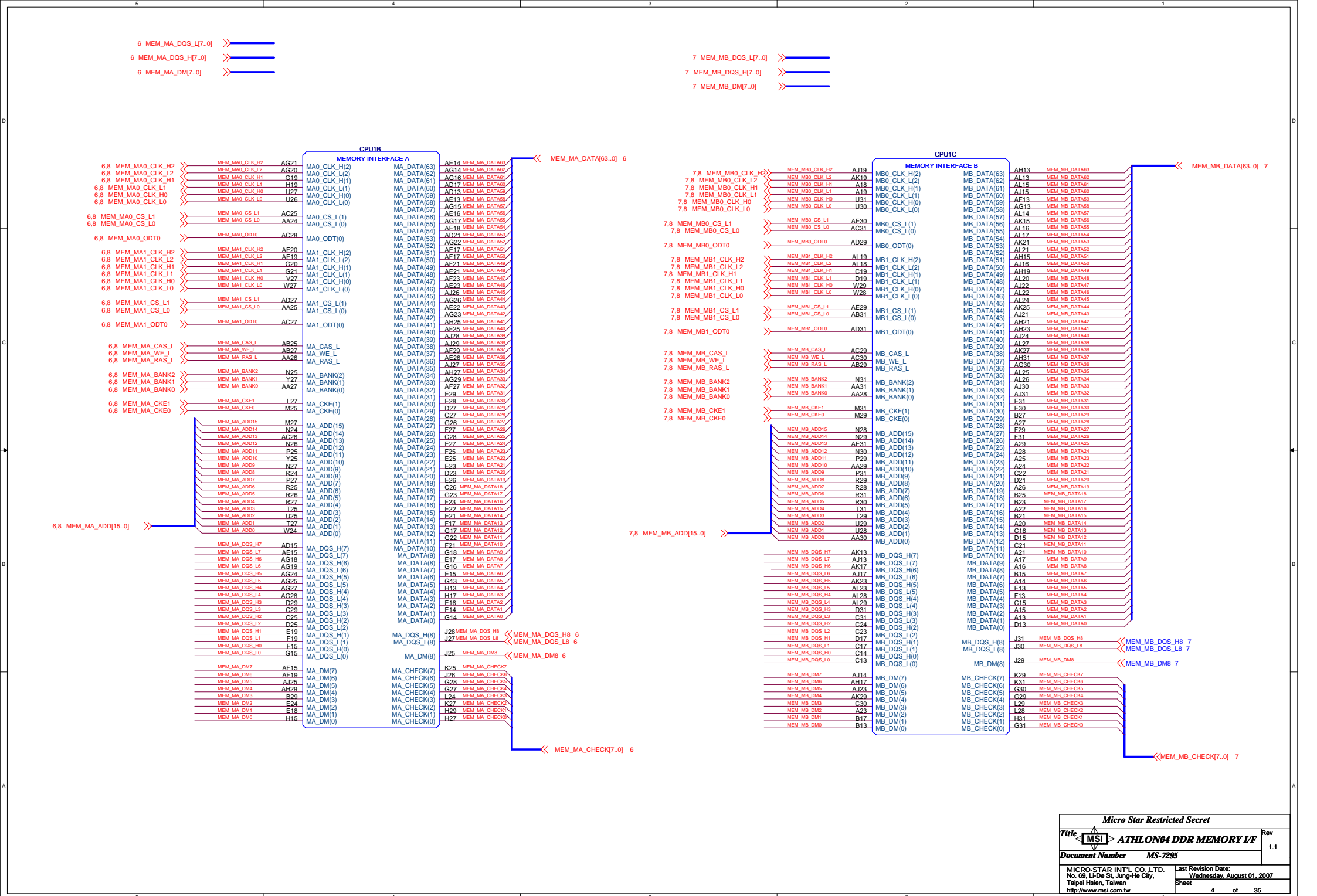
BLOCK DIAGRAM

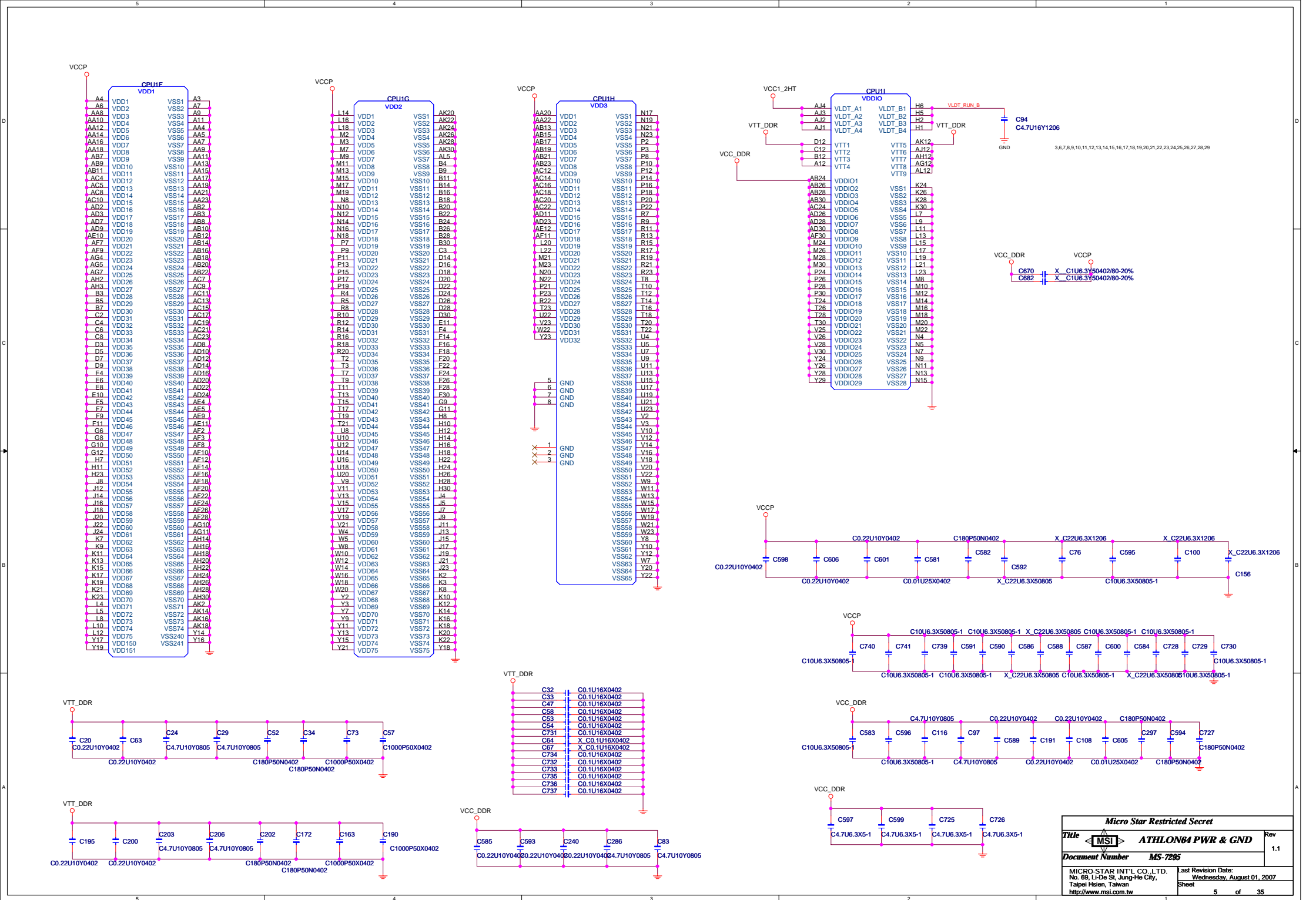


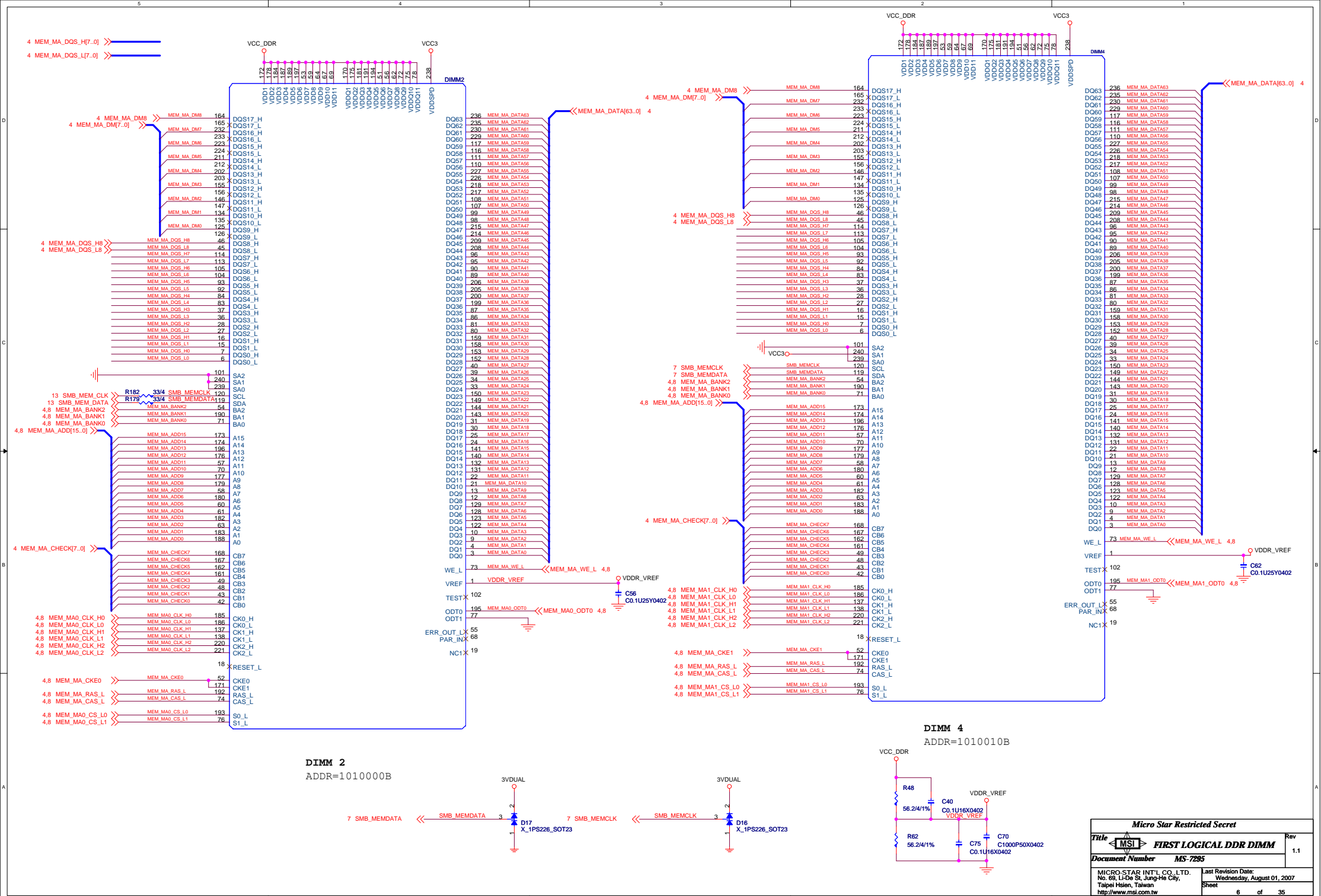


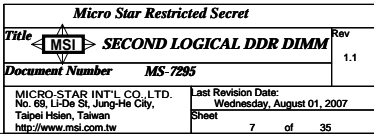
HT Bus Level shift

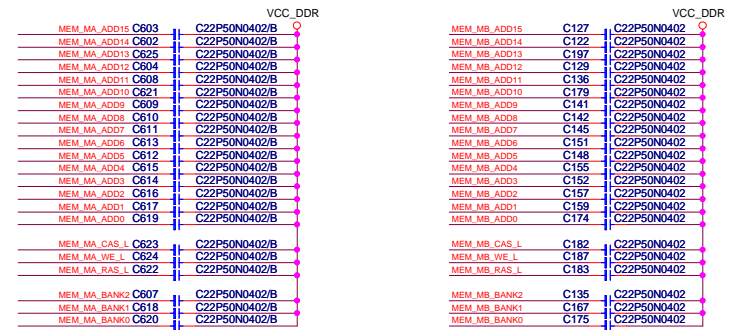
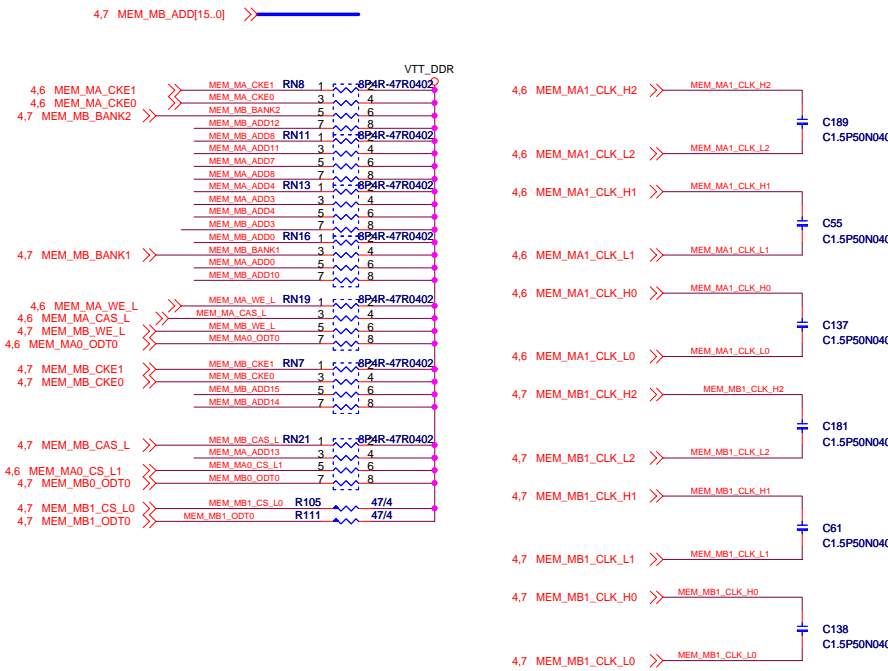
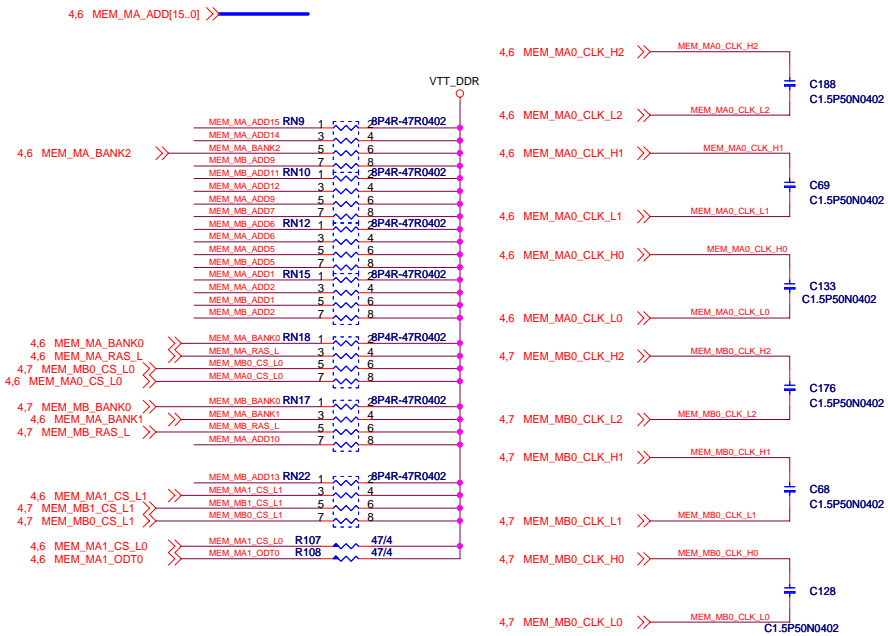






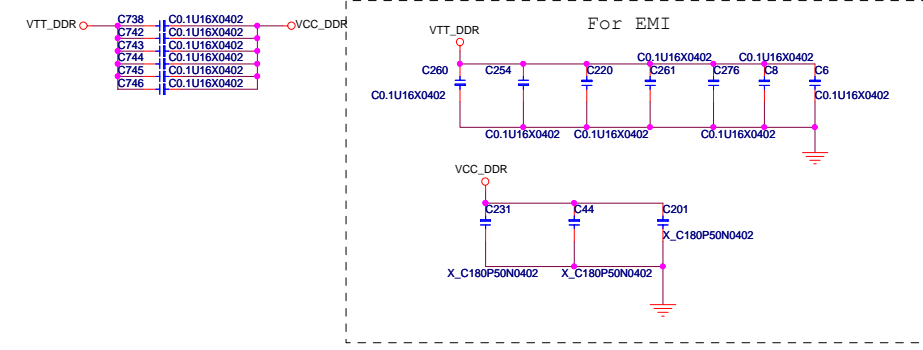
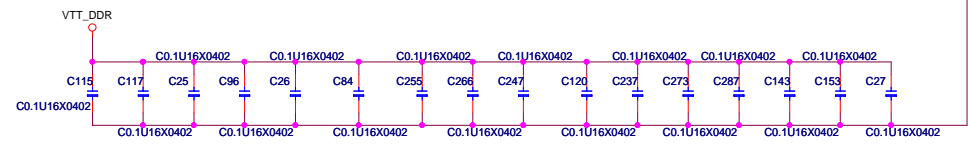
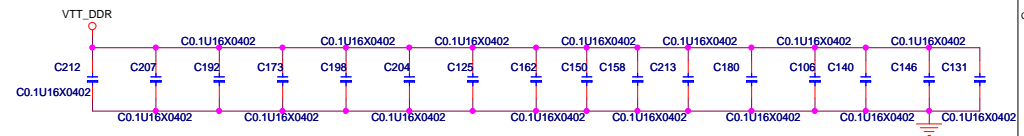


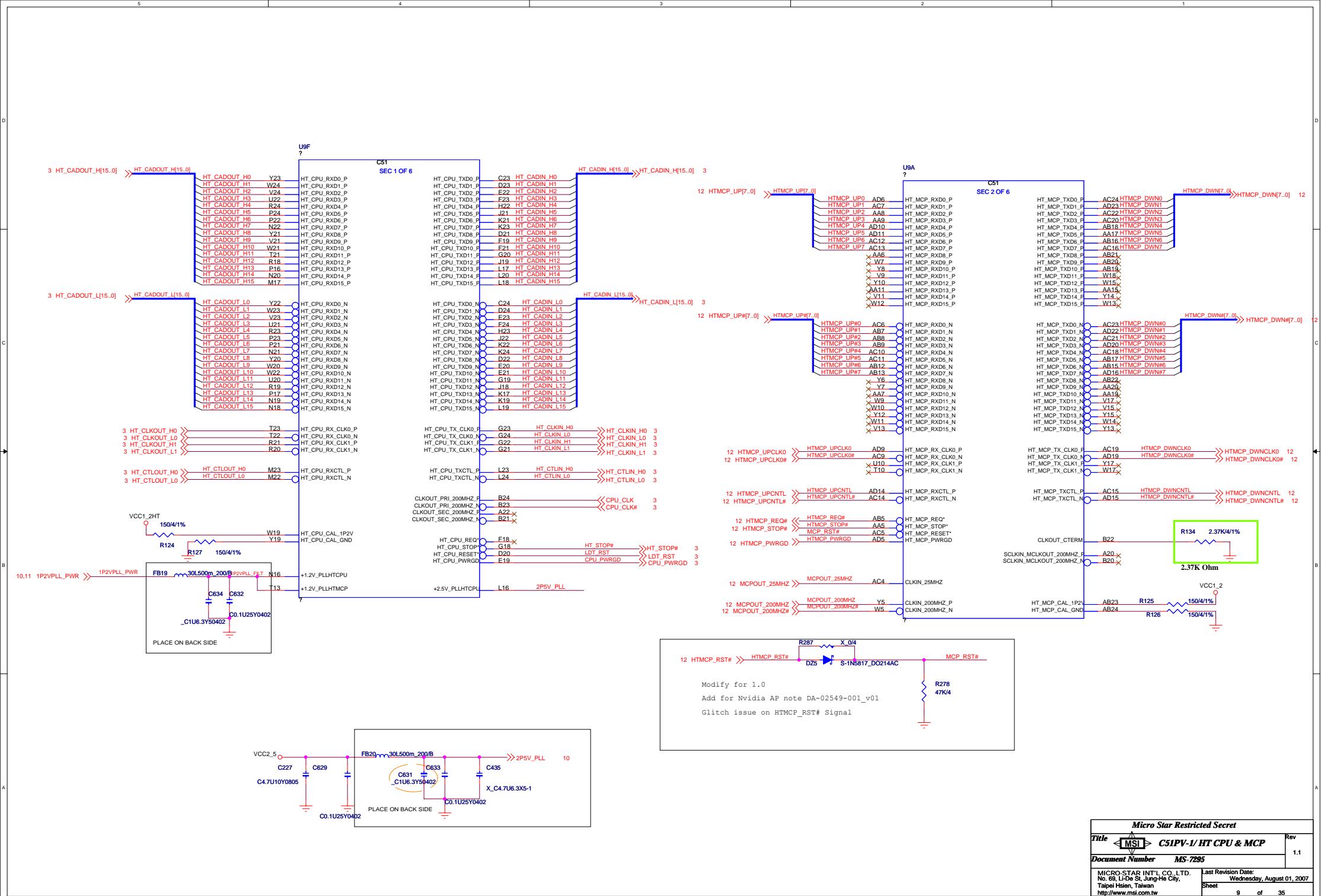


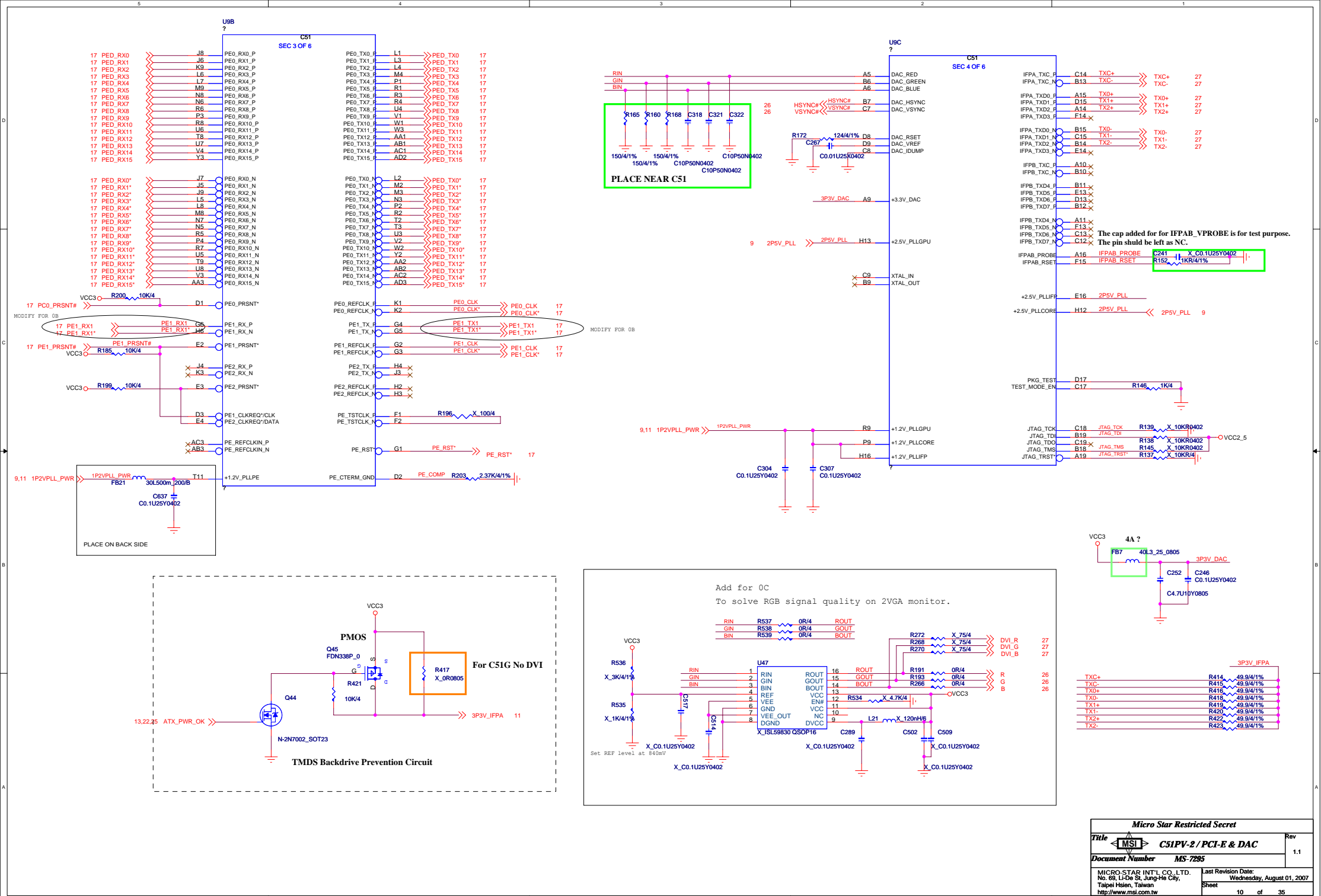


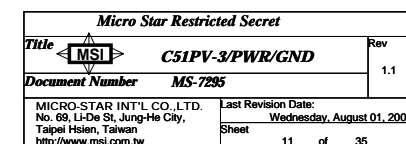
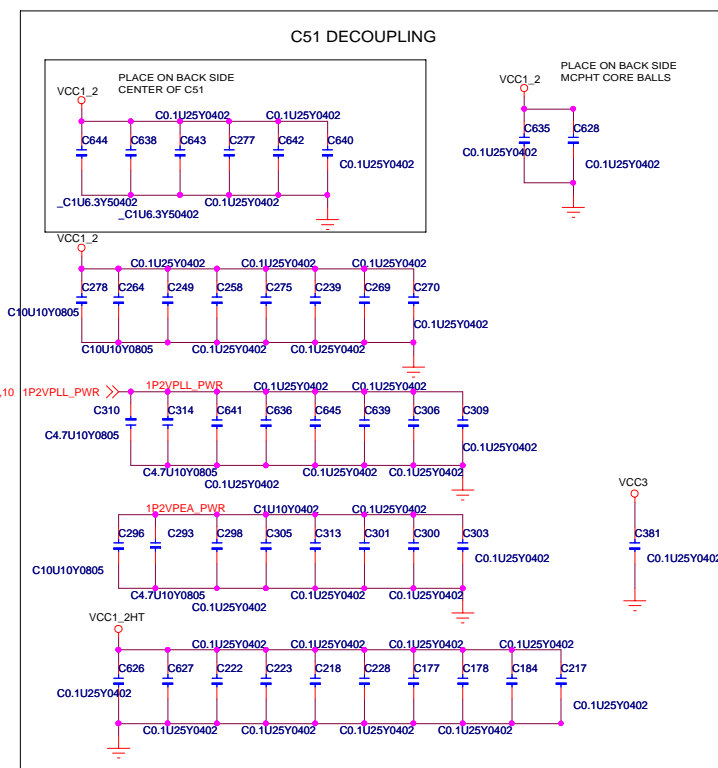
Decoupling Between Processor and DIMMs

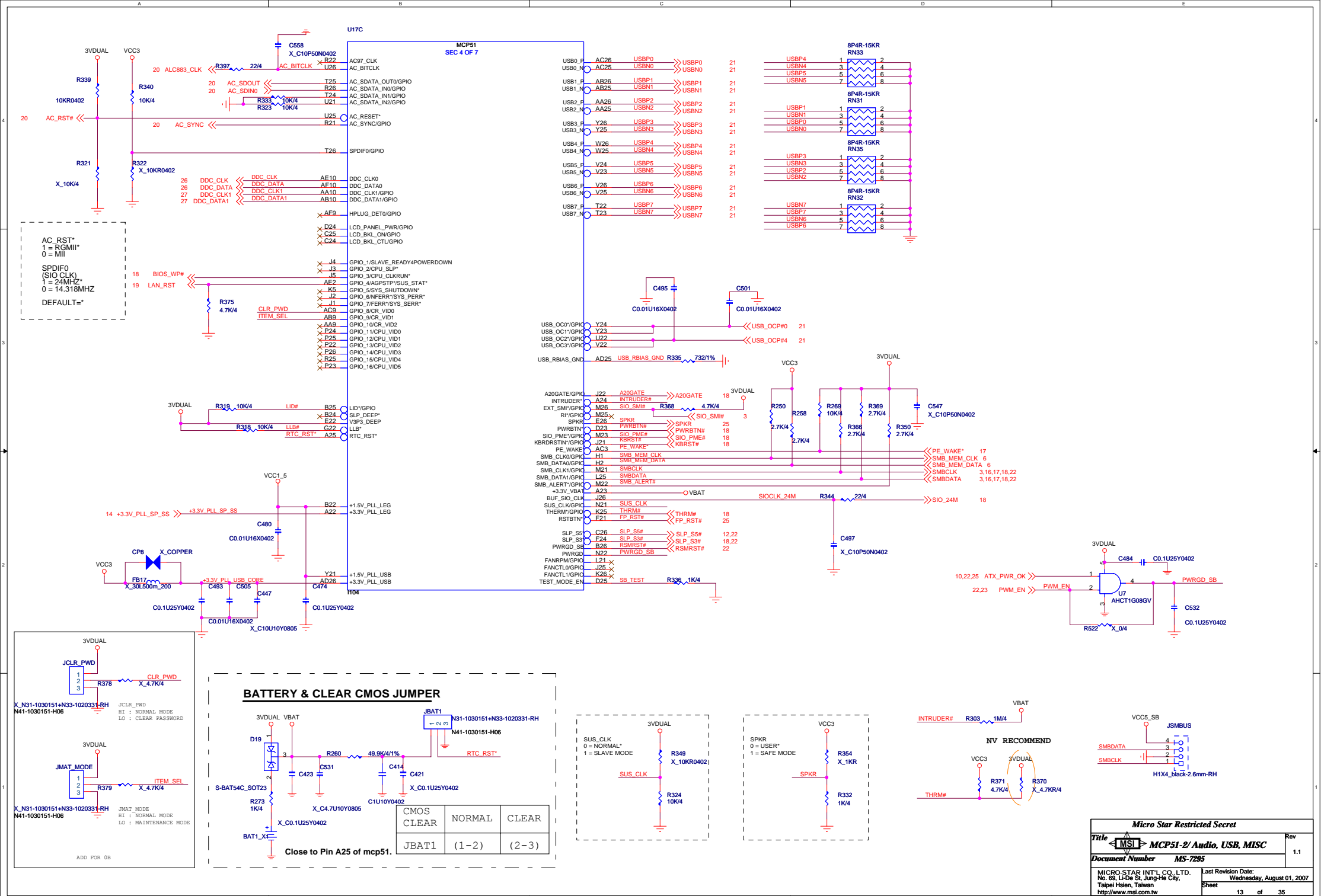
Layout: Spread out on VTT pour

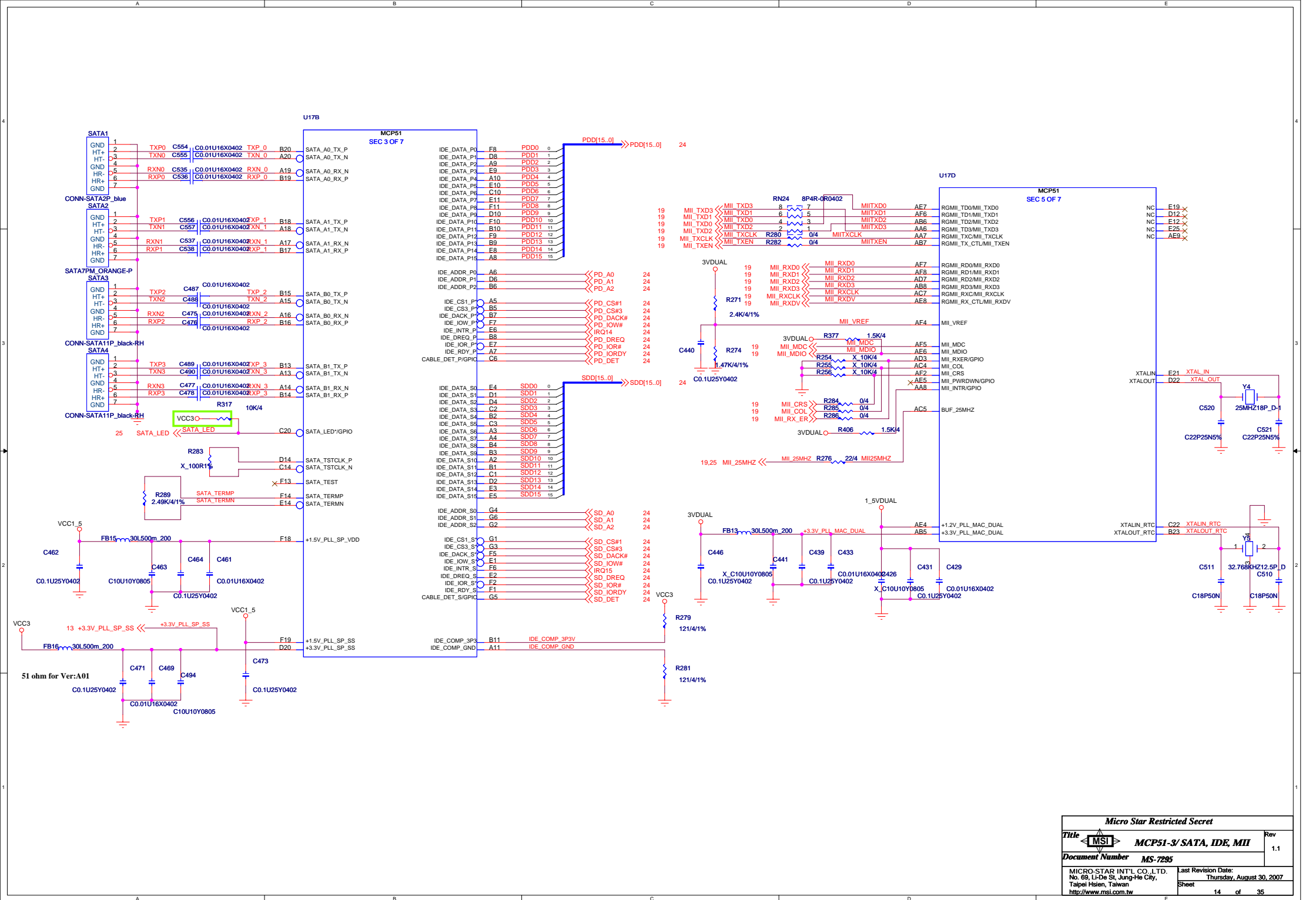


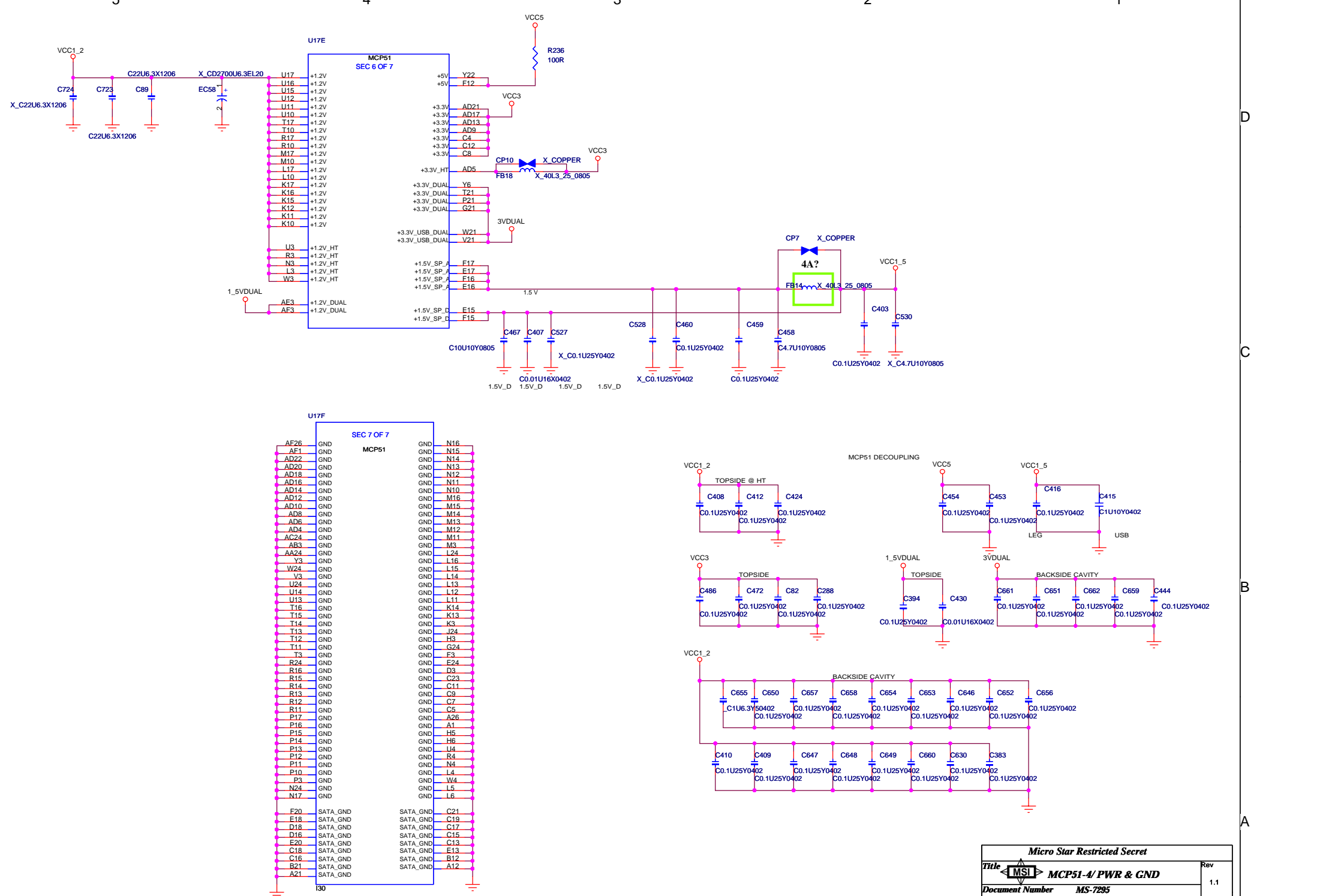






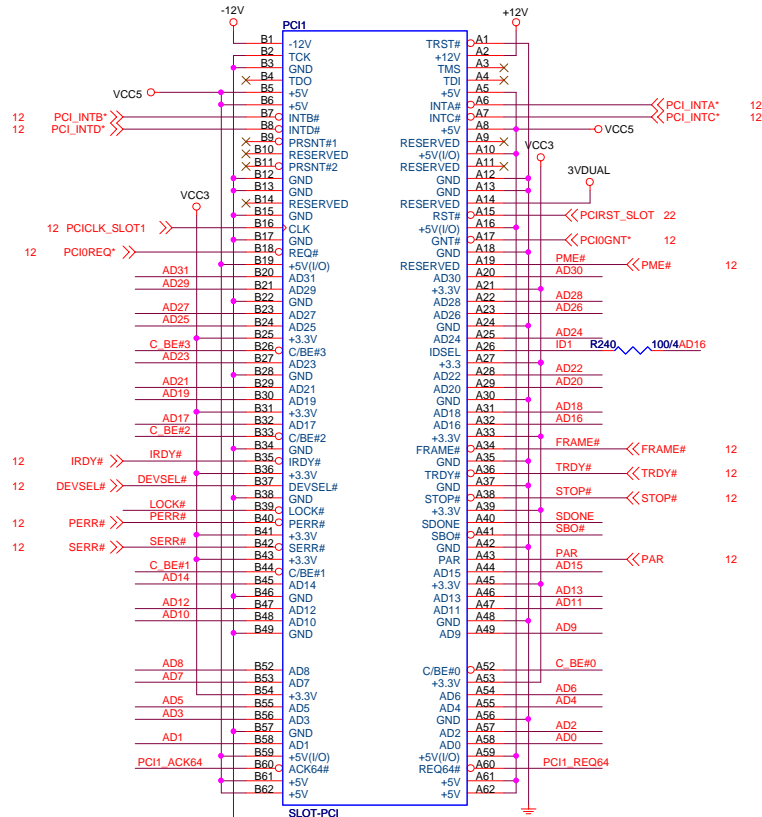






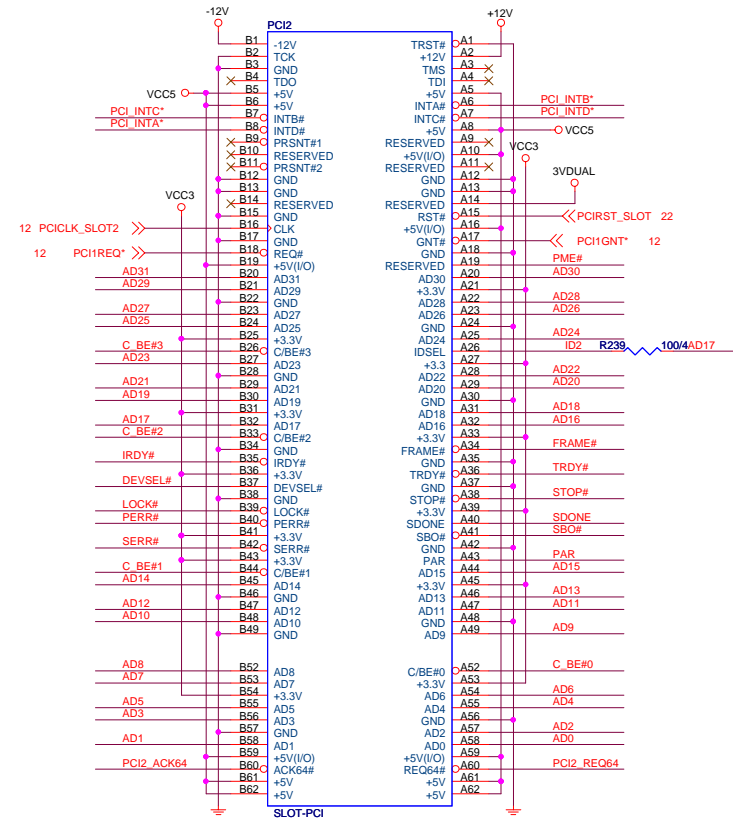
12 AD[31..0] >> AD[31..0]
12 C_BE#[3..0] >> C_BE#[3..0]

PCI SLOT 1 (PCI VER: 2.3 COMPLY)



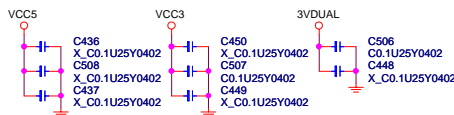
IDSEL = AD16
MASTER = PCI1REQ*
PCI1GNT*

PCI SLOT 2 (PCI VER: 2.3 COMPLY)

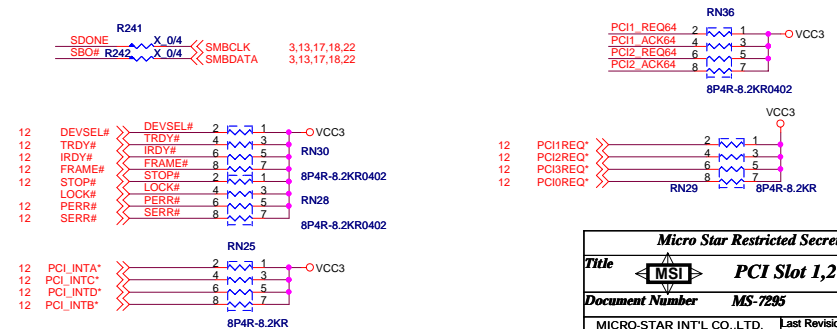


IDSEL = AD17
MASTER = PCI2REQ*
PCI2GNT*

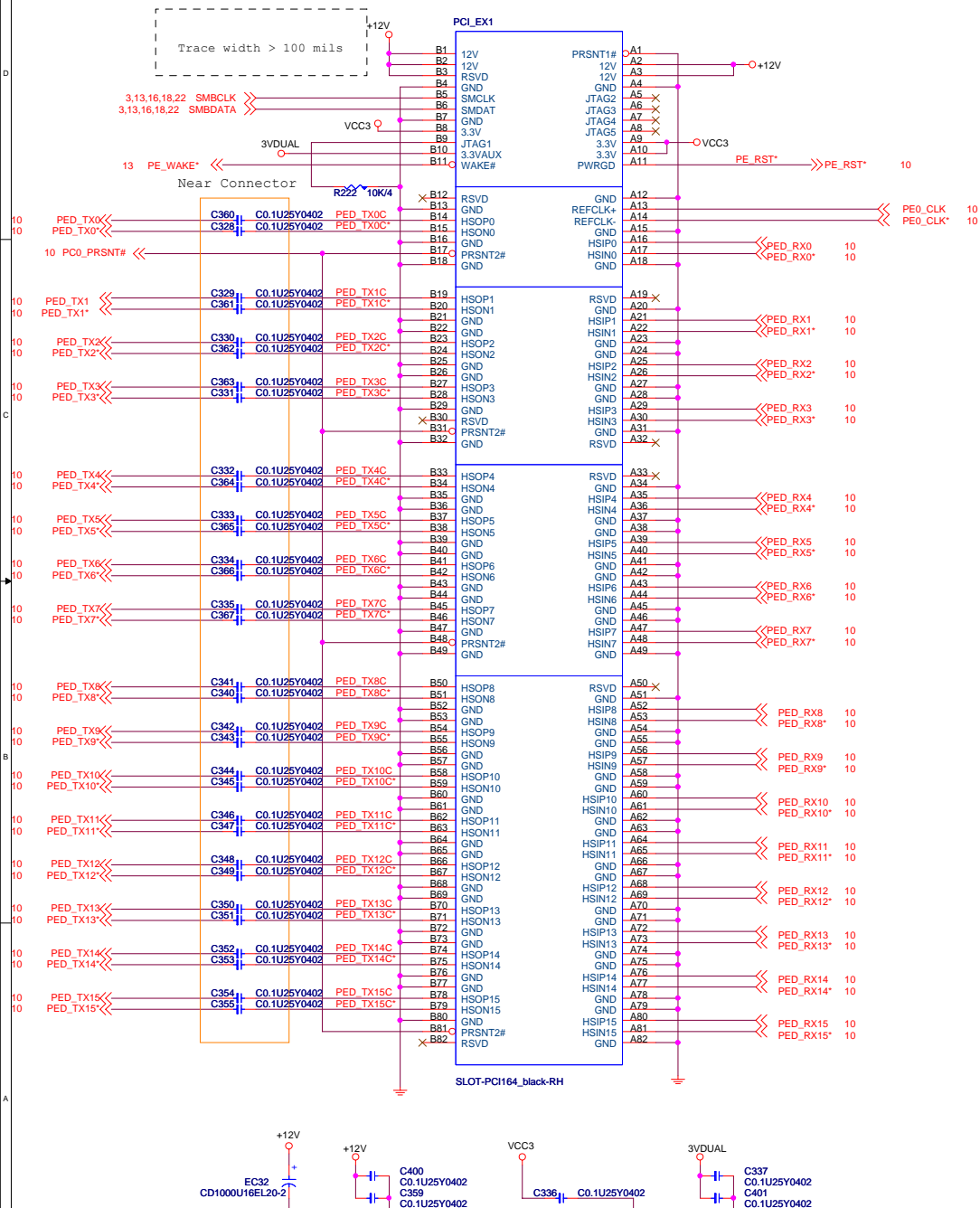
PCI SLOT DECOUPLING CAPACITORS



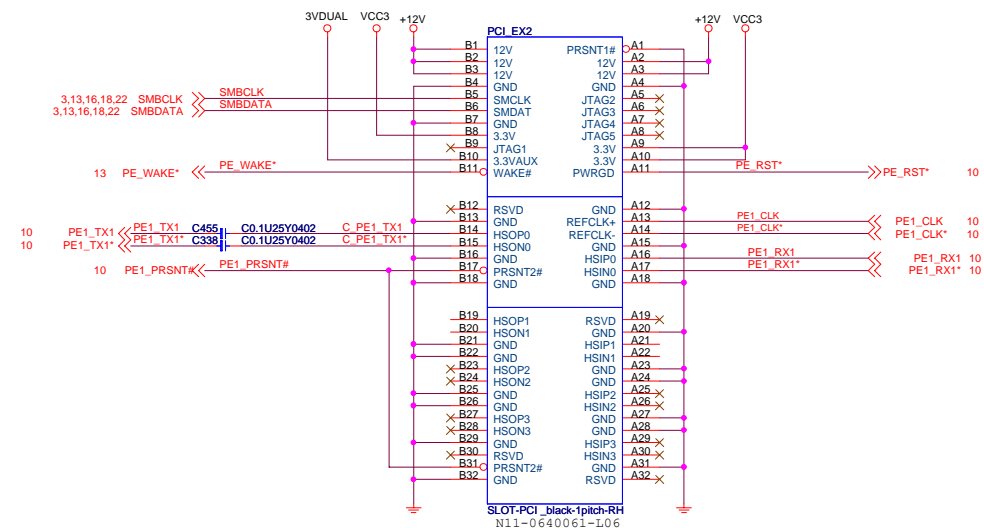
PCI PULL-UP / DOWN RESISTORS



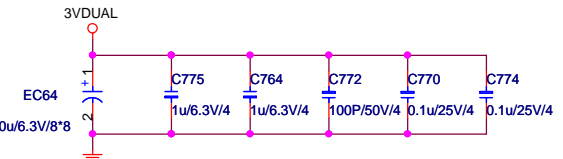
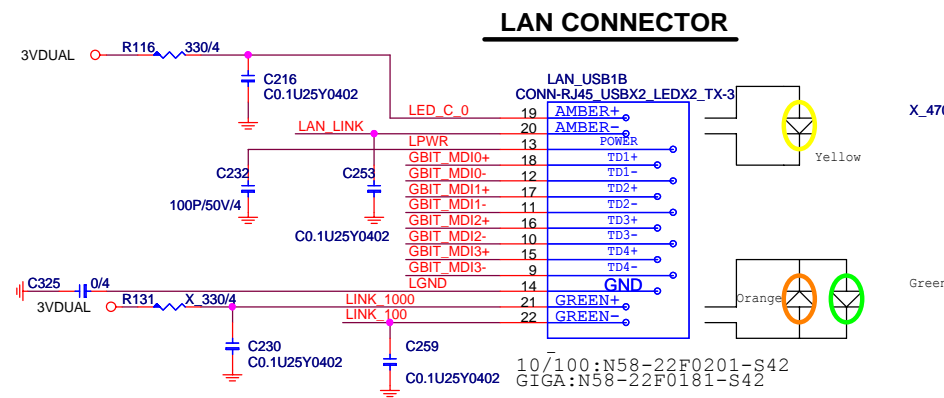
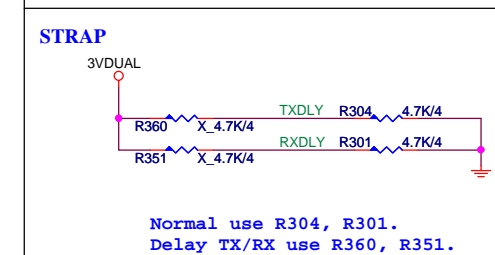
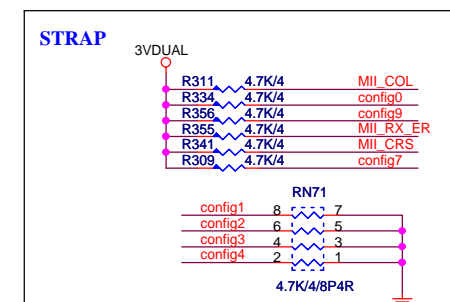
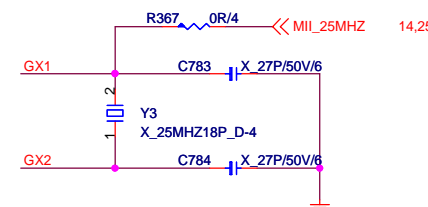
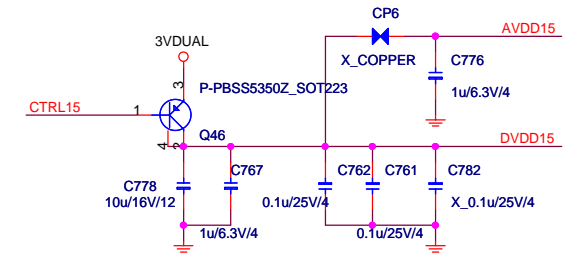
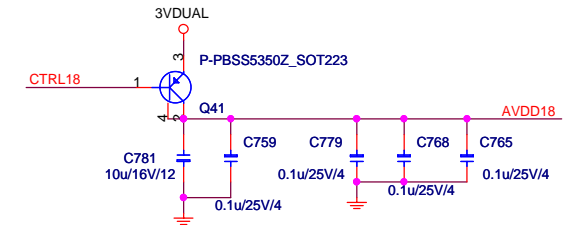
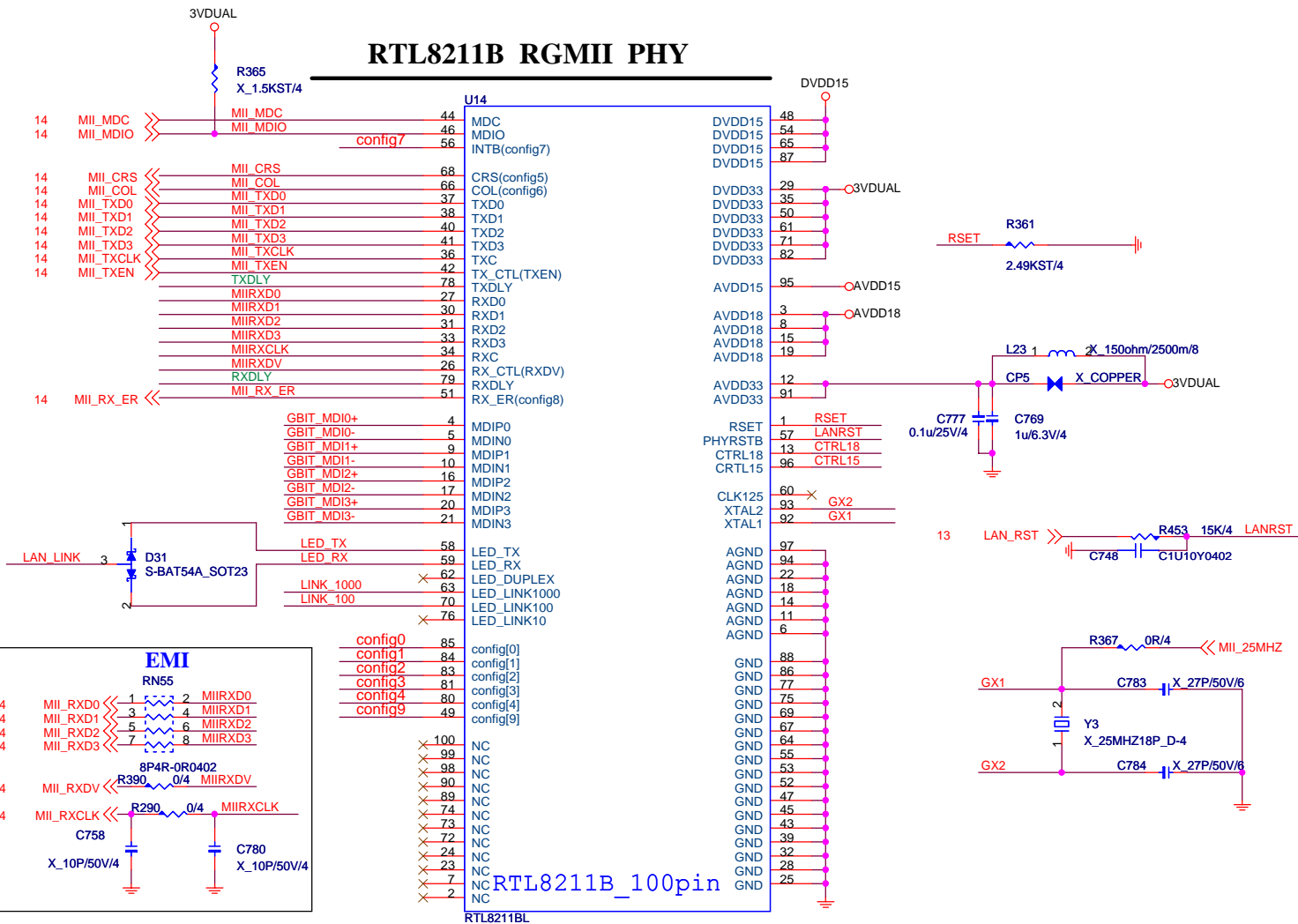
PCI EXPRESS_16



PCI EXPRESS x4-PORT



RTL8211B RGMII PHY

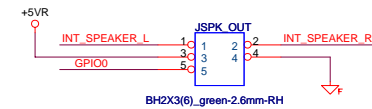
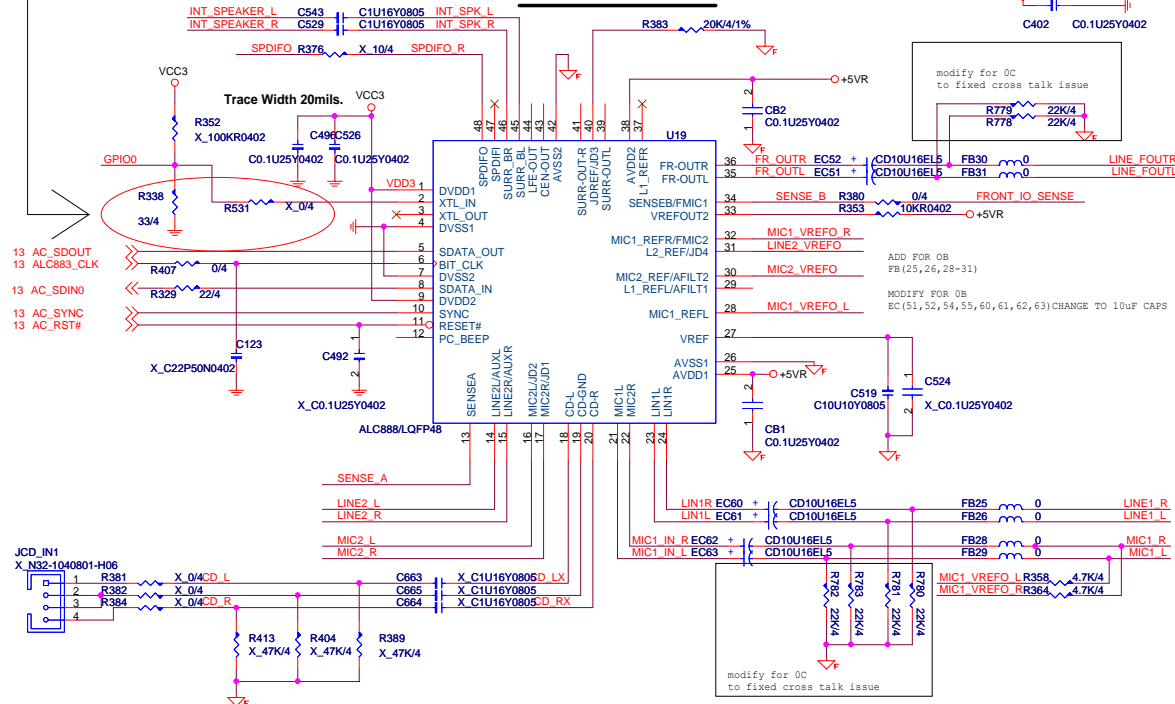


For Giga-bit Lan		
SPEED/LINK	LEFT	RIGHT
LINK	YELLOW	OFF
10 MBPS	YELLOW	OFF
100 MBPS	YELLOW	GREEN
1000 MBPS	YELLOW	ORANGE

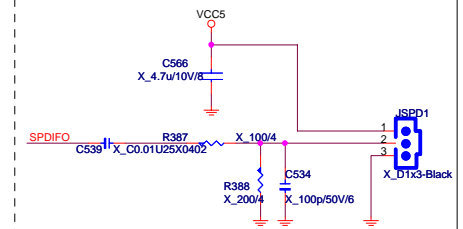
2005/7/18
Modify internal speak shutdown pin to low
1. Remove R531
2. Change R338 resistor value from 2Kohm to 33ohm

Because the internal speak is low active (if GPIO0 is low level then internal speak enable). But GPIO0 default state was hi. When used Vista O.S and without Realtek driver, the GPIO0 can not be control to low. So it will disable the internal speak.

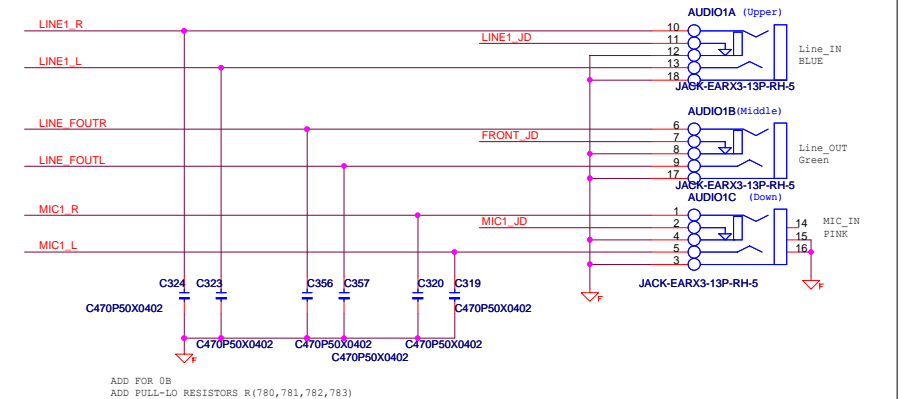
ALC888 CODEC



SPDIF OUT

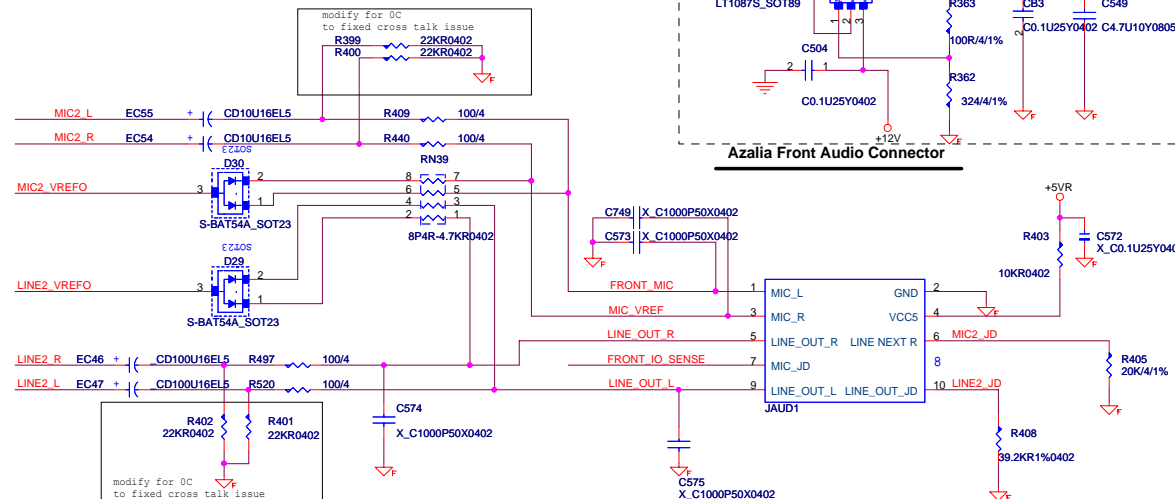


Rear audio jack

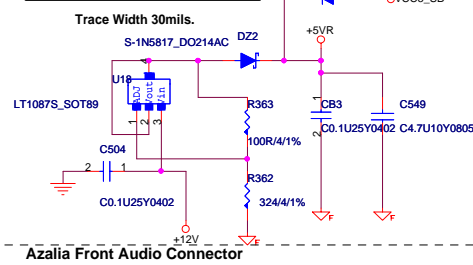


Speaker Out Decoupling

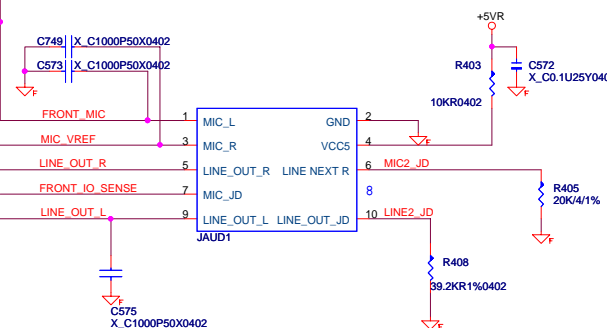
Place those component close to audio connector.



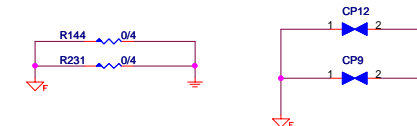
AUDIO CODE REGULATORS



Azalia Front Audio Connector



EMI Solution



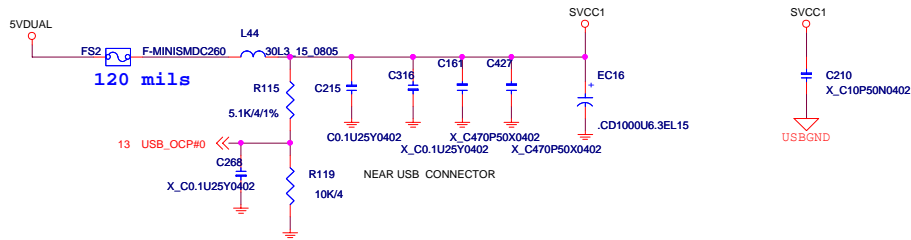
ALC888 JACK DETECT



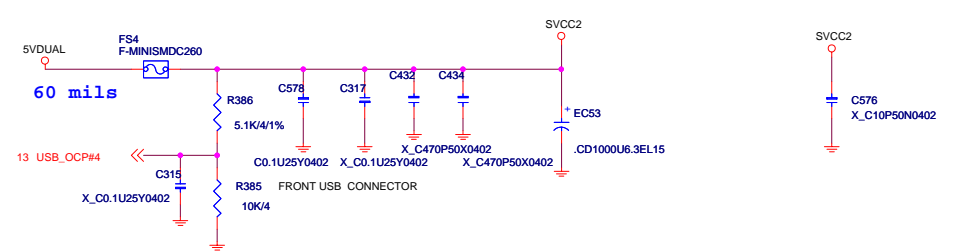
Closer to Codec.

MSI MICRO-STAR INT'L CO., LTD.			
Azalia & Interanl SPK			
Size	Document Number	Rev	
	MS-7295	1.1	
Date:	Wednesday, August 01, 2007	Sheet	20 of 35

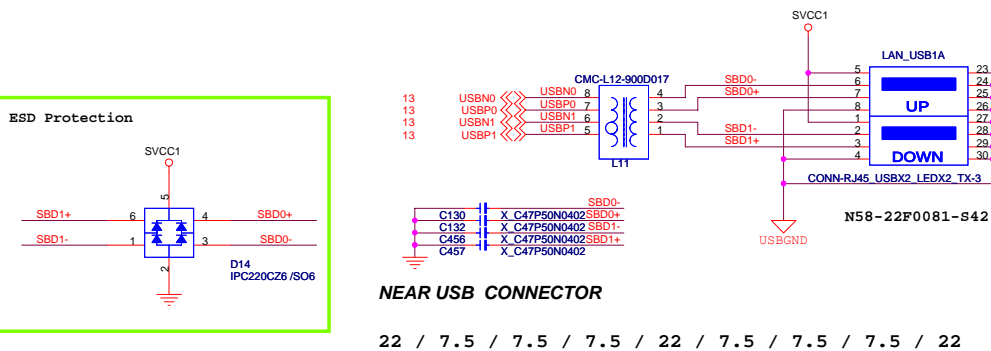
POWER CIRCUIT FOR USB PORT 0,1,2,3



POWER CIRCUIT FOR USB PORT 4,5,6,7

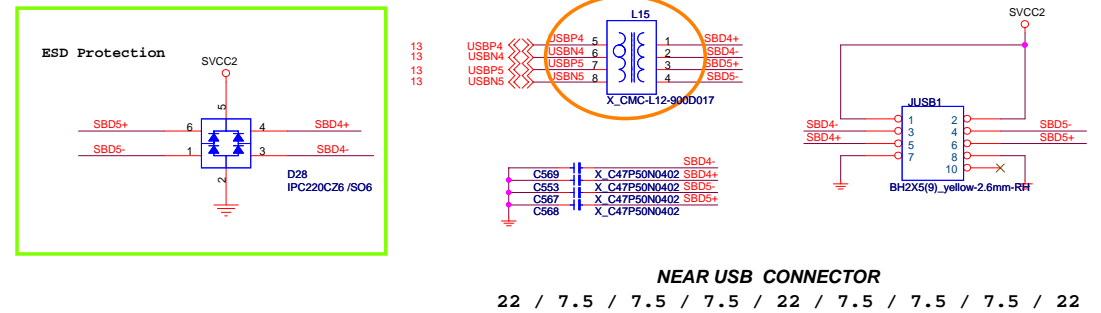


REAR PANEL USB CONNECTOR FOR USB PORT 0,1

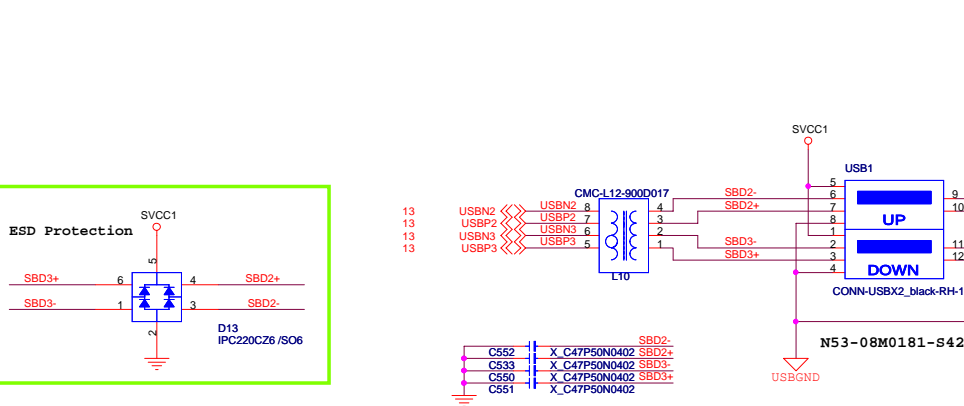


FRONT PANEL USB CONNECTOR FOR USB PORT 4,5

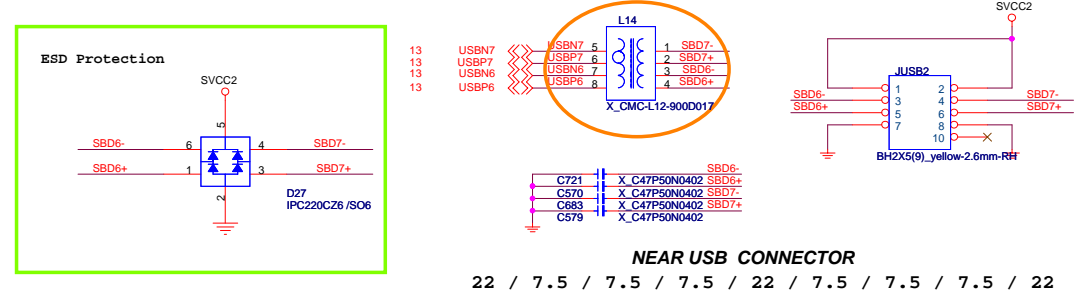
Reserved, can be taken off riser card within bead



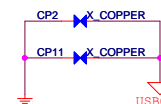
REAR PANEL USB CONNECTOR FOR USB PORT 2,3



FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

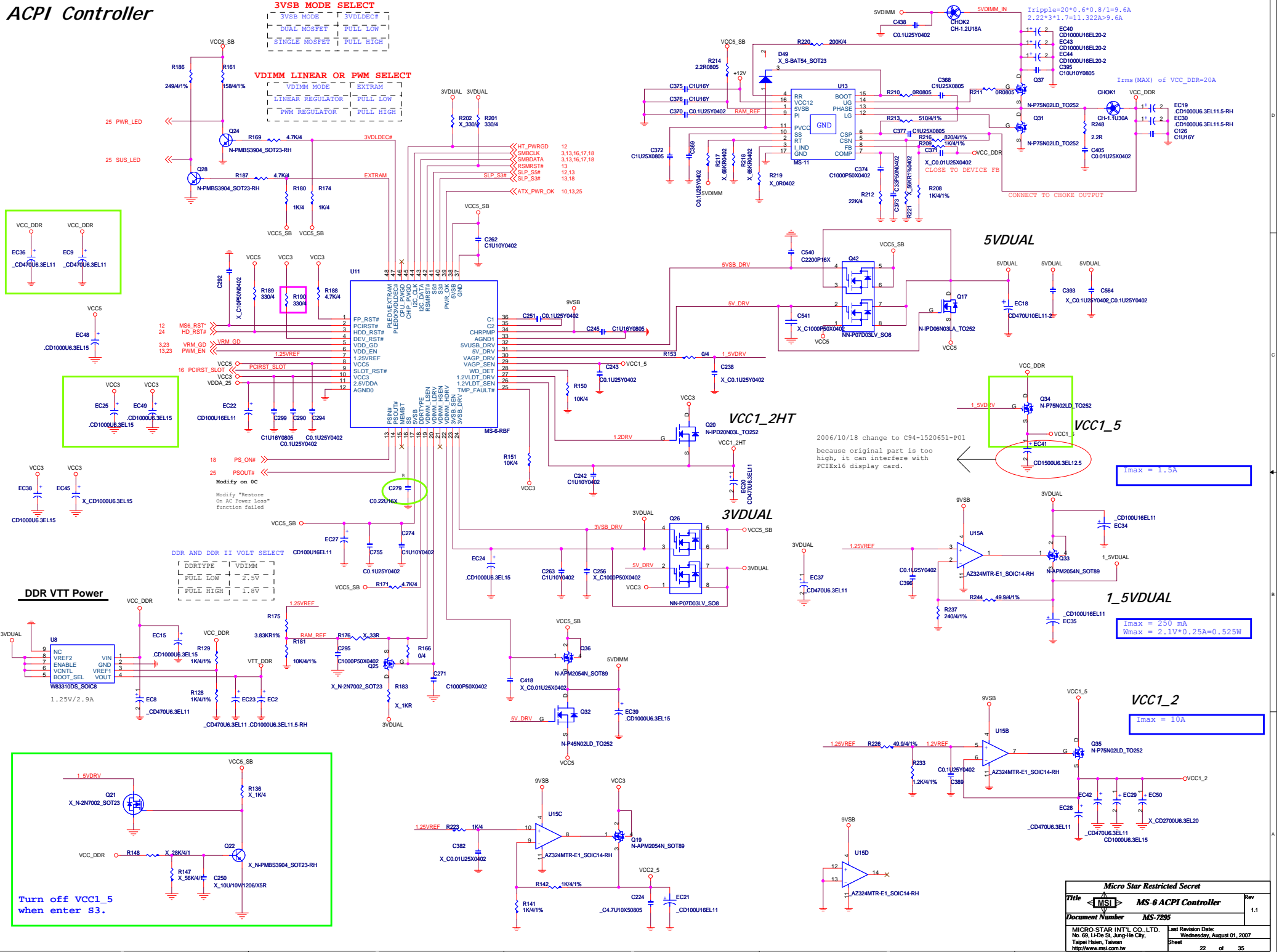


EMI TEST



MSI		MICRO-STAR INT'L CO., LTD.	
Title		USB CONNECTORS	
Size	Document Number	MS-7295	
Date:	Wednesday, August 01, 2007	Sheet	21 of 35

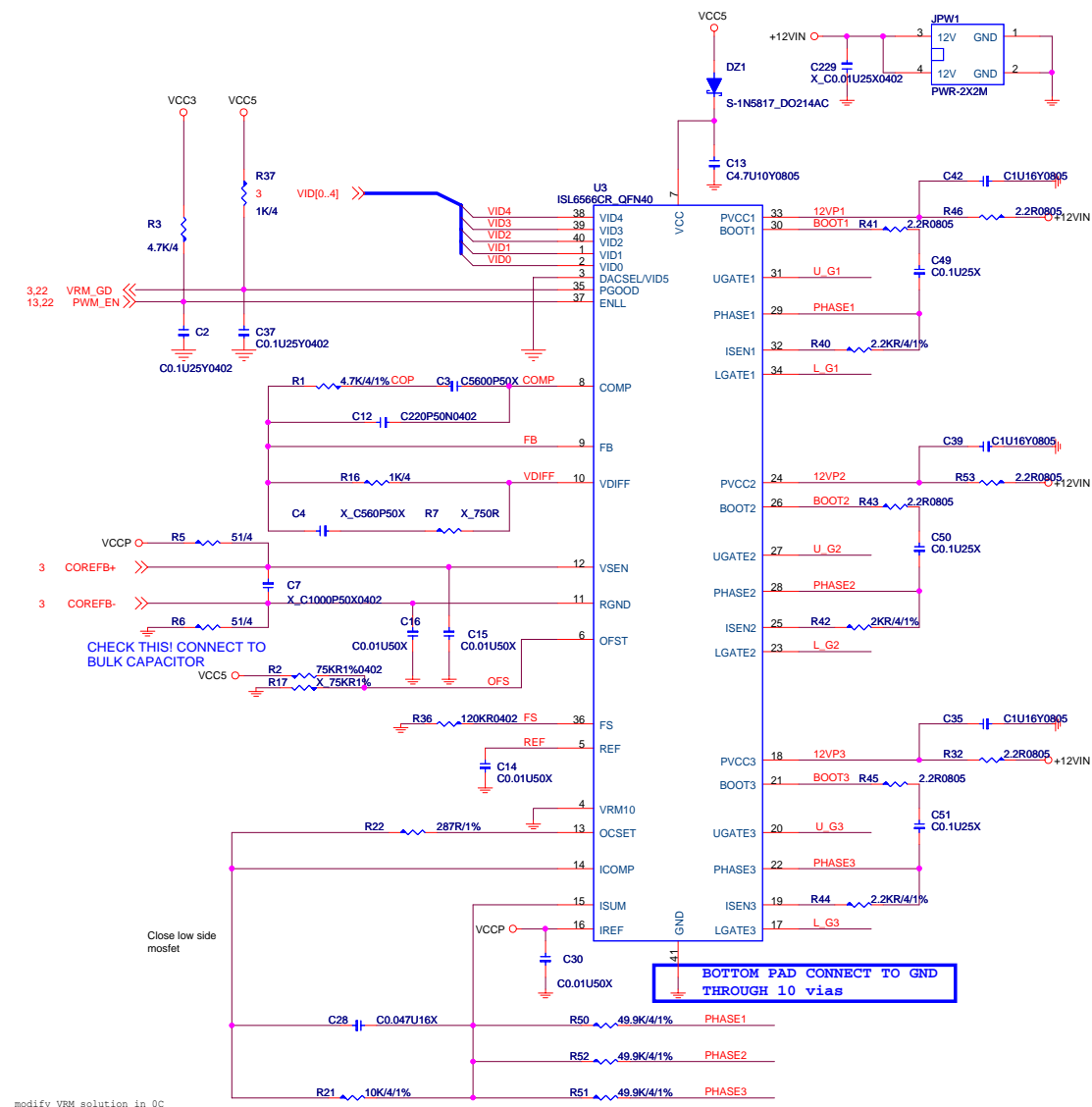
ACPI Controller



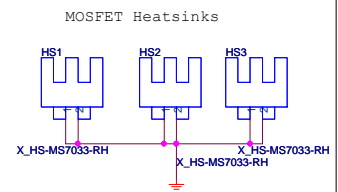
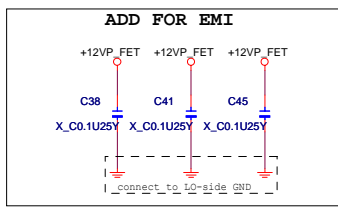
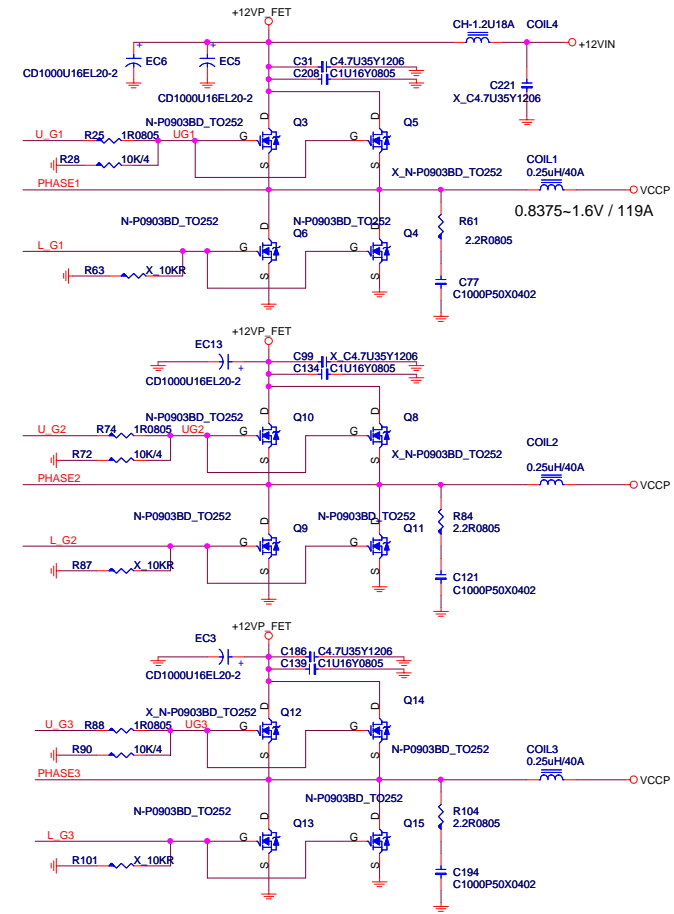
Voltage Regular Module

IPF06N03LA
C100U2SP
.CD3300U6.3EL25
560u_2.5V
1800UF/6.3V
0.6uH/40A
CH-1.2U18A

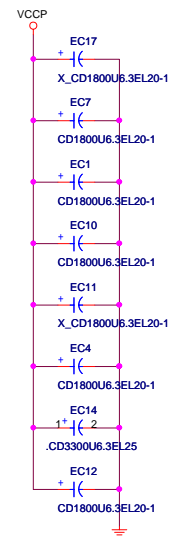
Rds(on)=8.7mΩ (@4.5V, 30A), Vgs(ON)=1.2~2V, Id=50A, Ciss=3110pf, Qg=10nC, Vds=25V, Vgs=±20V
ESR<13mΩ, Ripple cur.<2.7A, LC<12uA, 105C
ESR<12mΩ, Ripplecur.<2800mA, 105C, longlife3000hrs, KZJSeries
ESR=6mΩ, Ripplecur.=4400mA, Lc.<500uA, 105C/2000hrs
ESR<12mΩ, Ripplecur<2350mA, 105C, longlife change from 2000hrs to 3000hrs ,KZJ series
0.6u/20%, Isat=40A, Rdc=1.2m ohm, PEW wire
1.2u/20%, Dip-2/vertical 7.5mm, 1.2ψ/5.5turns, 18A



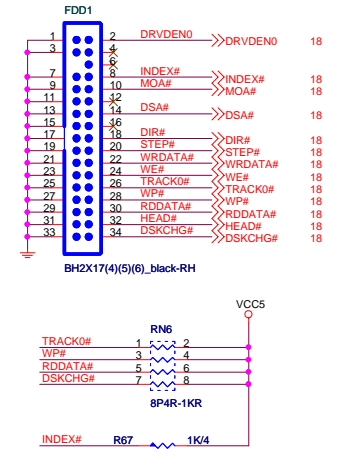
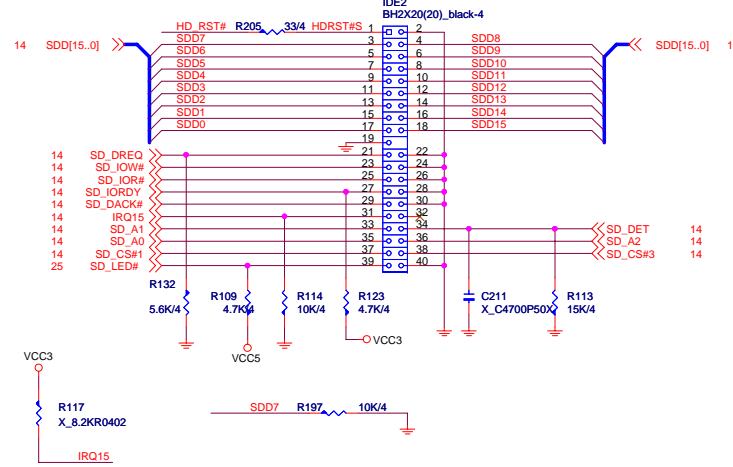
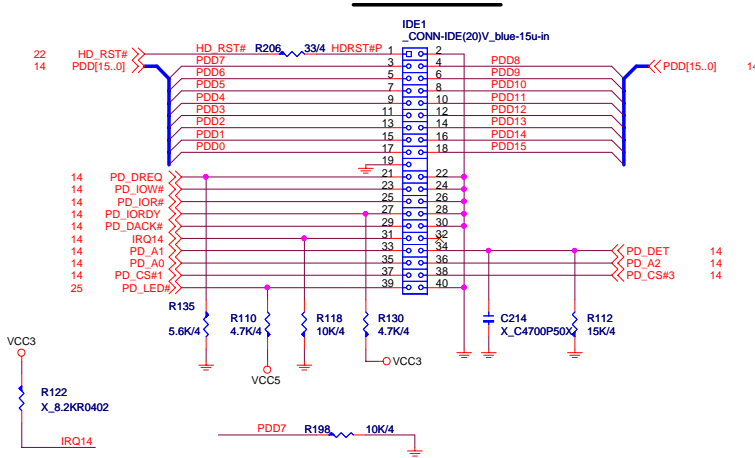
modify VRM solution in OC
R2 change to 75K ohm 14
R36 change to 120K ohm
R42 change to 2K ohm
remove Q5,Q8,Q12 in bom
Q(4,6,9,11,13,15) change to NIKOS 0903BDG (D03-0903BDB-N03)



EL Capacitors

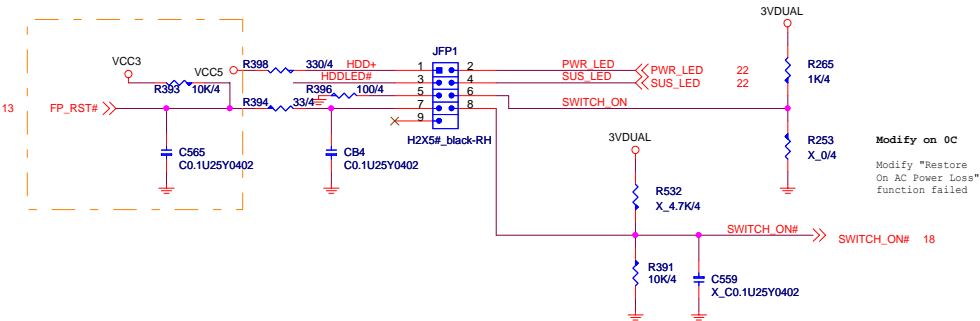


MICRO-STAR IN'L CO., LTD.			
Title			
Intersil 6565ACV 3 Phase			
Size	Document Number	Rev	
	MS-7295	1.1	
Date:	Wednesday, August 01, 2007	Sheet	23 of 35

[illegible]

ATX connector / Front Panel

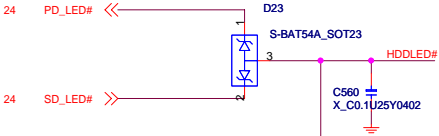
Intel Front Panel



DHG : Low active
R256->N/I
R391->N/I
R253->00HM
R532->4.7K

EHG : High active
R256->1K
R391->10K
R253->N/I
R532->N/I

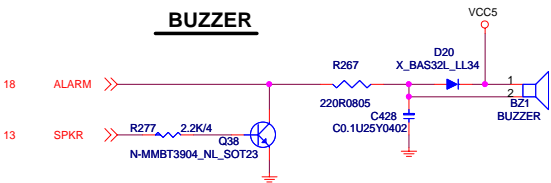
IDE LED



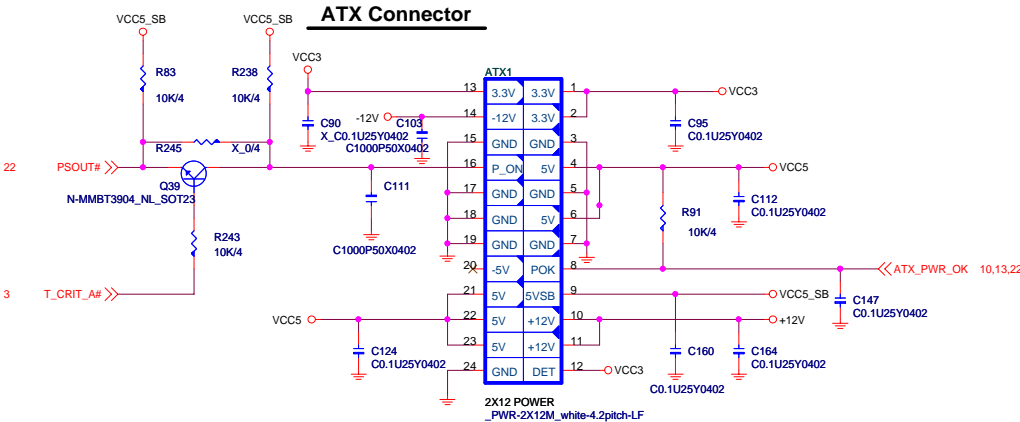
SERIAL ATA LED



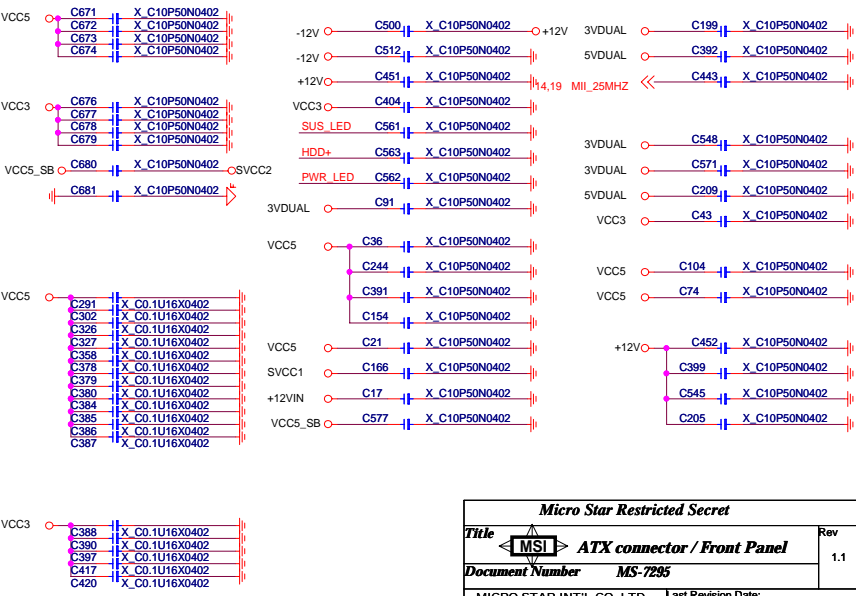
BUZZER



ATX Connector

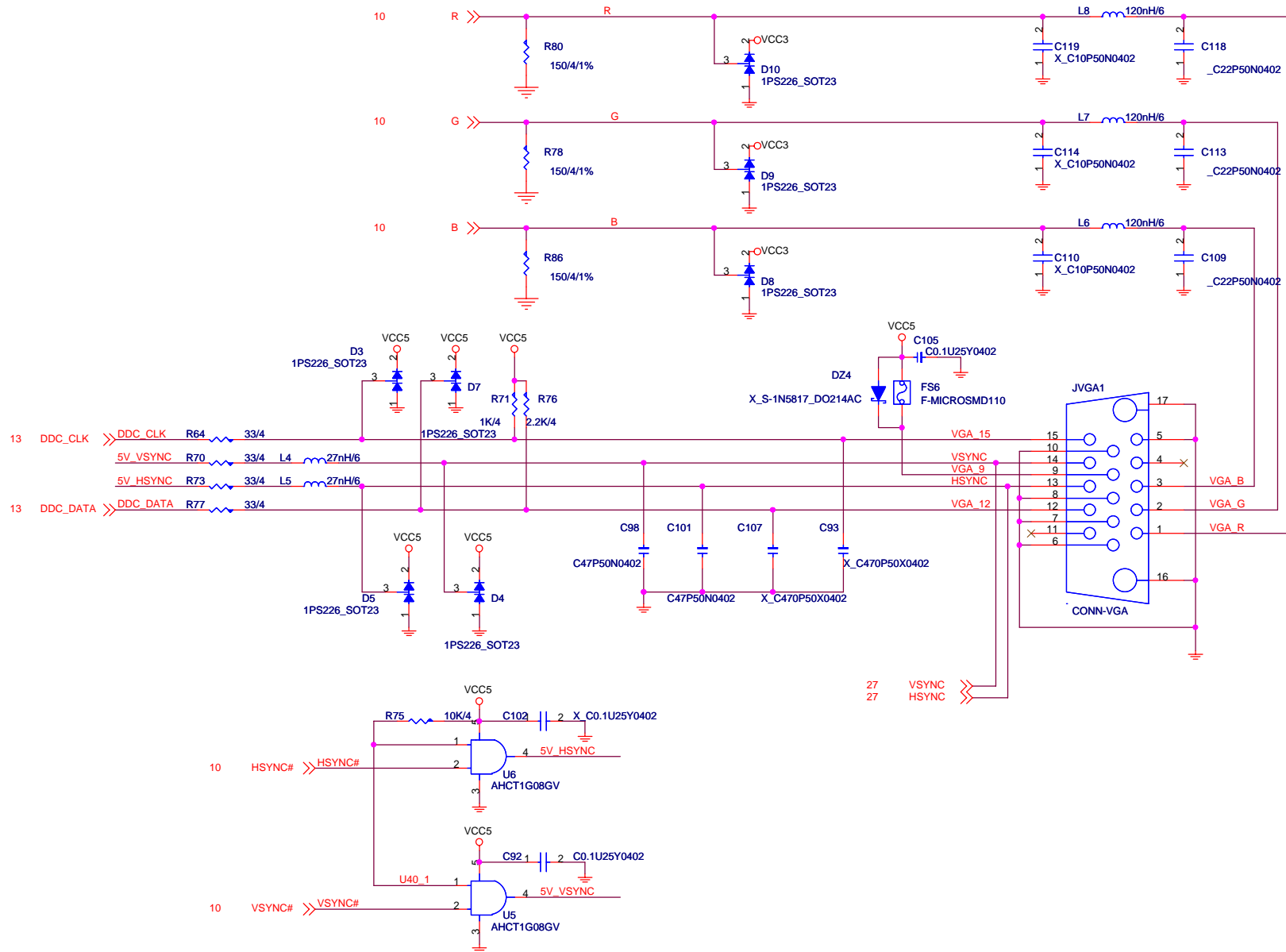



For EMI

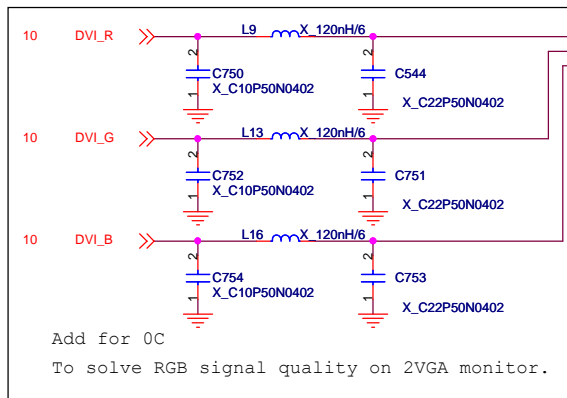
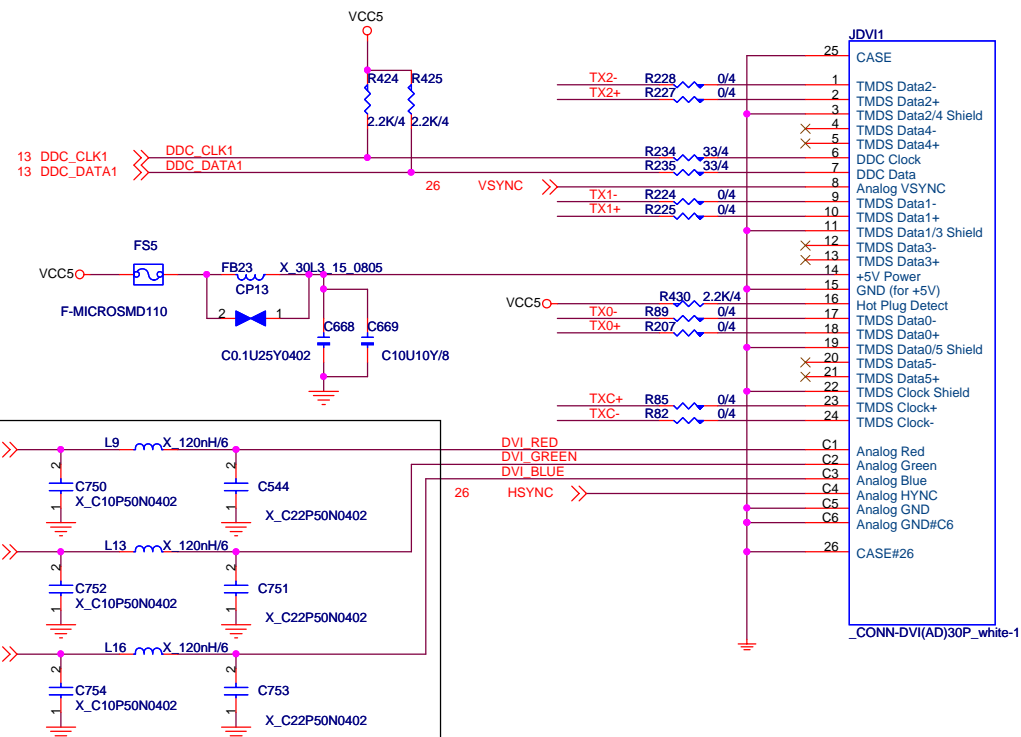
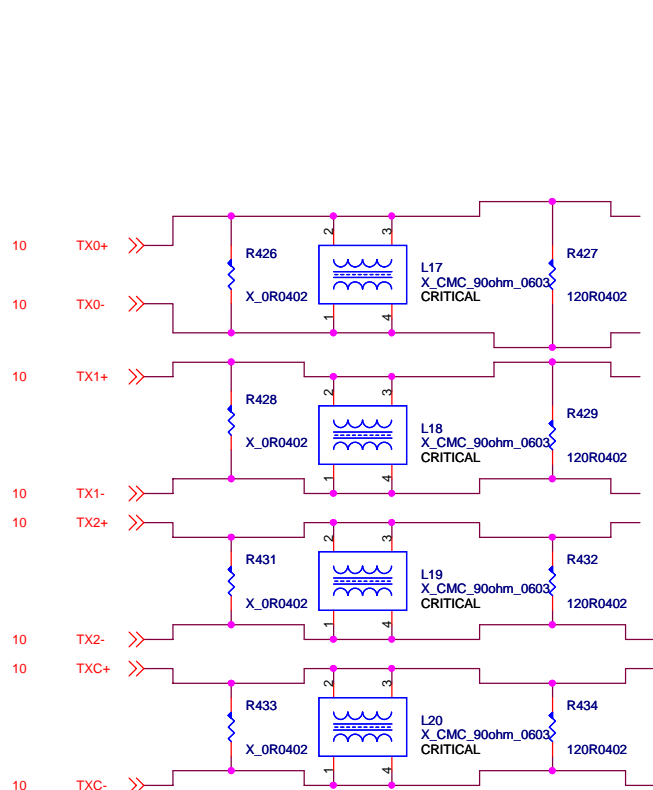


VGA CONNECTOR

close VGA connector

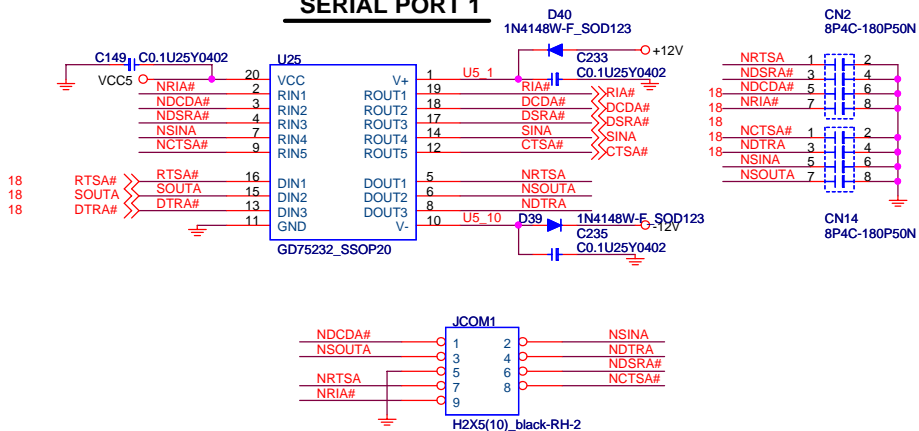


<i>Micro Star Restricted Secret</i>			
Title <div></div> VGA CONNECTOR	Rev 1.1		
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Sheet		26	of 35

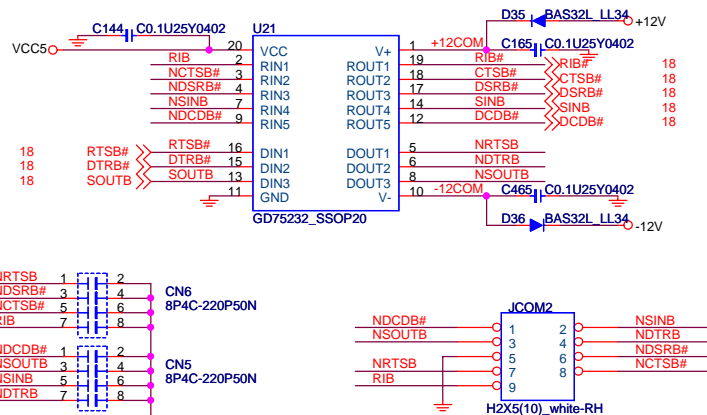


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Last Revision Date: Wednesday, August 01, 2007		
Sheet 27 of 35		

SERIAL PORT 1

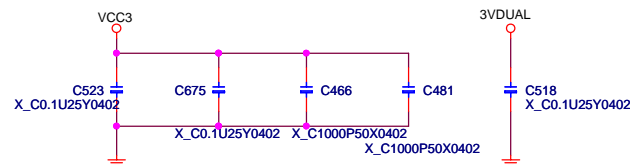
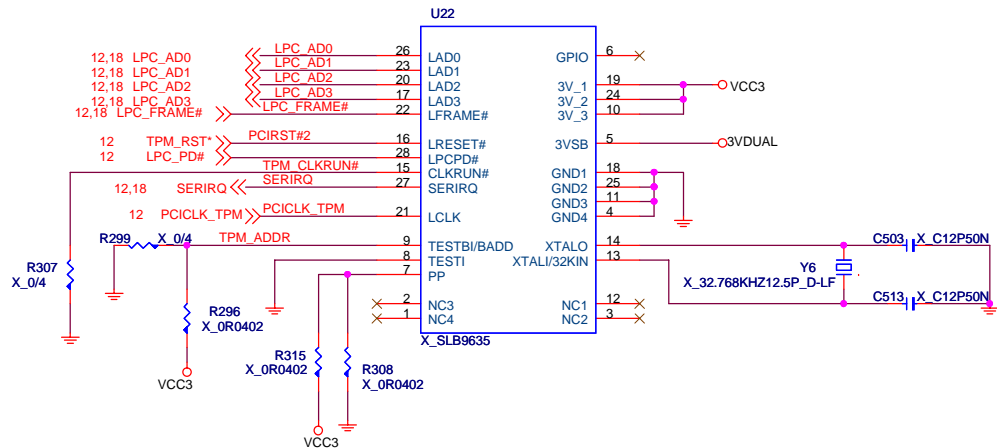


SERIAL PORT 2

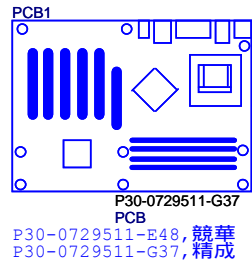
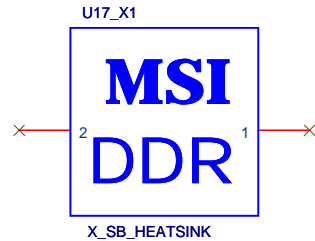
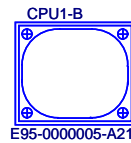
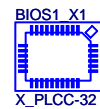
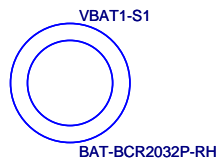
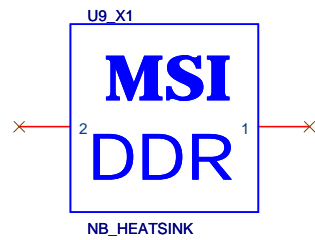


TPM 1.2

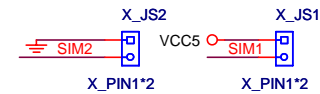
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		MICRO-STAR INT'L CO., LTD.	
Title: COM PORTS & TPM 1.2			
Size:	Document Number: MS-7295		Rev: 1.1
Date: Wednesday, August 01, 2007		Sheet: 28 of 35	

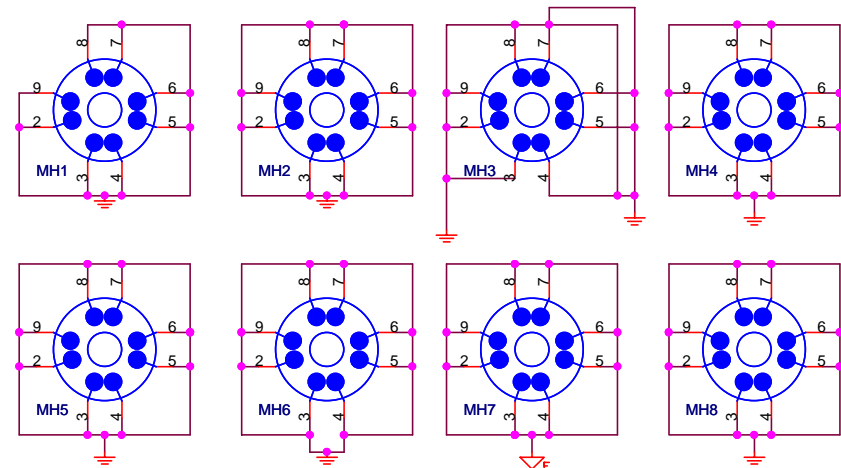
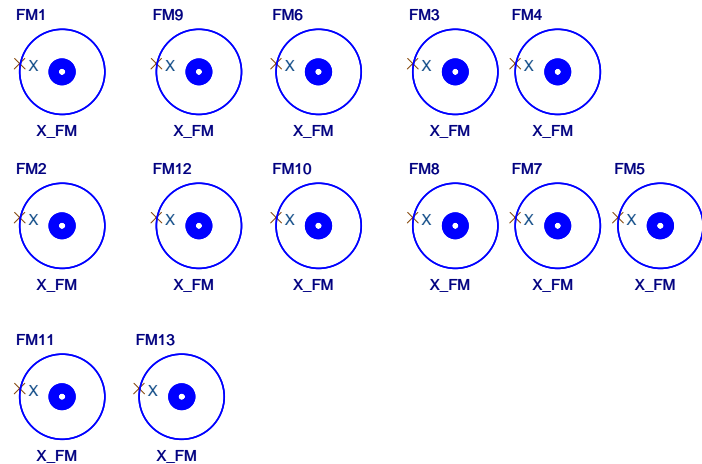


Simulation



Mounting Holes

Optics Orientation Holes



Micro Star Restricted Secret		
Title	TEST POINTS & PCB	Rev
Document Number	MS-7295	1.1
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Wednesday, August 01, 2007 Sheet
		29 of 35

ver : 0A data : 2006 / 03 / 23

Modify for AMD check list


Page03 : HT_STOP_L, LDT_RST_L and CPU_PWRGD_L have 330 ohm pullup resistors (RN5). The recommend value for the pullup resistors is 300 ohms (5%).
Page03 : Add level shifting to RESET_L . modify R23 pin1 & J1 pin24 from LDT_RST_L to LDT_RST.
Page05 : change caps(C34,C52,C202,C172) value to 180-pF.
Page03 : Change the part of L2 position , change the part to L02-4008044-C08.
Page03 : Add a level shift circuit for AMD test tool.
Page05 : Add 2x 1uF caps (C670 & C682) from VDDIO to VCCP .
Page05 : Add a fuse (FS3) for PS2 power .

Modify for nVidia check list

Page26 : Remove D21,D31, R285,R440 for MCP51 A03 .
Page26 : Add a poly fuse (FS6) for VGA power.
Page27 : Reserved 0Ω series resistor close to DVI connector.
Page14 : Add 10 kΩ pull-down resistors for MII_RXER,MII_COL,MII_CRS
Page14 : Add a Pull-up resistor(R377=1.5 kΩ) to RG/MII_MDIO
Page13 : Change strap pin (AC_RESET#) to pull up , to select RGMII mode.
Page15 : Add a bypass cap (C425 0.01uF) for 3P3_IFPA_L .
Page27 : Add damping resistors (R234 & R235 33ohm) for DDC_CLK1 & DDC_DATA1 .
Page19 : Add a damping resistor (R526 0ohm) for RG/MII_INTR .
Page21 : Reserved bypass caps (C161 , C427 , C432 & C434 470pF) for SVCC1 & SVCC2 .
Page16 : Add Pull-up resistors (RN36= 8.2KΩ) for ACK64# & REQ64# (PCI solt pin)
Page14 : Reserved bypass cap (C494 10uF) for +3.3V_PLL_SP_SS
Page15 : Reserved bypass caps (C527 & C528 0.1uF) for +1.5V_SP_A & +1.5V_SP_D
Page15 : Add a damping resistor (R236 100ohm) for +5V
Page15 : Rerserved a ferrite bead (FB18) for +3.3V_HT
Page14 : Reserved bypass cap (C530 4.7uF) for +1.5V_SP_A
Page13 : Reserved bypass cap (C531 4.7uF) for +3.3V_VBAT
Page09 : Reserved bypass cap (C435 4.7uF) for 2P5V_PLL
Page13 : Reserved bypass cap (C447 10uF) for +3.3V_PLL_USB_CORE
Page26 : Reserved bypass caps (C107 & C93 470pF) for DDC_CLK & DDC_DATA .
Page21 : Reserved bypass caps (47pF) for USB1.1 mode .
Page22 : Reserved bypass caps and place near Q35 (EC50 2700uF) for VCC1_2.
Page11 : Reserved bypass caps (C80 & C81 22uF) for VCC1_2.
Page11 : Reserved bypass caps (C85 47uF) for 1P2VPPLL_PWR.
Page15 : Reserved bypass caps place near MCP51(EC58 & EC59 2700uF) for VCC1_2.
Page15 : Reserved bypass caps place near MCP51(C88,C89,C723 & C724 22uF) for VCC1_2.
Page26 : Reserved a diode(DZ4 1N5817) co-lay with FS6 for VGA power.

Modify for MSI

Page03 : Modify LM90 circuit , THERMDA_CPU connected to D+ & THERMDC_CPU connected to D- .

Micro Star Restricted Secret				
Title		HISTORY FOR 0A	Rev	
			1.1	
Document Number		MS-7295		
MICRO-STAR INT'L CO., LTD. No. 68, Li-De St, Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Wednesday, August 01, 2007		
		Sheet	30 of 35	

ver : 0B data : 2006 / 05 / 04

Modify for MSI

Page19 : Modify lan circuit (MII_RXD0~3)
Page10 : Modify PCI_EX2 CIRCUIT (PE1_RX1/PE1_RX1* & PE1_TX1/PE1_TX*)
Page13 : ADD JUMPER SELECT FOR CLEAR PASSWORD & MAINTENANCE MODE
Page20 : Modify codec circuit for co-lay ALC888

ver : 0C data : 2006 / 05 / 17

Modify for MSI

Page28 : Change JCOM1 color to black
Page21 : L10 & L11 change to common choke
Page23 : modify VRM solution
Page17 : PCI-express X16 CHANGE TO AUTOMATIC CLIP
Page21 : JUSB1 & JUSB2 change to 2*4pin header without housing
Page28 : JCOM1 change to black color
Page28 : JAUD1 change to blue color
Page30 : CPU retention module change vender to AVC
Page18,22,25 : Modify "Restore On AC Power Loss function" failed
Page10,27 : Add amplifier to solve RGB signal quality on 2VGA monitor.
Page22 : add EC49 & EC25 for VCC3

Modify for LAYOUT

1. Add mask on CPU screw and connect the shape to GND
2. FS3,EC46 move out the MH7 & MH1
3. Fix mechanical issue of audio caps
4. Modify VTT_DDR plane to 200mil (at least 200mil)
5. Modify CPU_VDDIOFB_H/L route to VCC_DDR power supply
6. Modify processor clocks route as 5mil trace with 5mil spacing
7. Modify data group signals failed length matching with clks
8. Modify MA-MEN_MB_DATA49 failed length matching

Modify for AMD

Page05 : Add C206 (4.7uF) for VTT_DDR

Modify for NECCI

Page20 : Codec change to ALC888
Page27 : DVI-I change DVI-D
Page10 : remove R,G,B amplifier

ver : 10 data : 2006 / 06 / 16

Modify for MSI

Page18 : Modify R533 pull-up power to VCC5_SB (PS_ON#)
Page09 : Add Nvidia AP note DA-02549-001_v01, to solve Glitch issue on HTMC_P_RST# Signal
Page21 : Remove USB bypass caps.
Page28 : Remove TPM function.
Page08 : Add EMI solution.
Page30 : Add mylar on U23.
Page22 : Del EC45 1000uF cap and add 1000uF cap on EC38.
Page05 : Add 3 22uF 0805 caps on C(590,595,739) .
Page20 : Modify internal speak shutdown pin state to low.

Modify for LAYOUT

Modify internal power layer for Vista.

ver : 10 data : 2006 / 10 / 18

Mechanical issue on Bogota

Page22 : EC41 change to C94-1520651-P01
because original part is too high, it can interfere with PCIEx16 display card.

ver : 11 data : 2007 / 07 / 19


Spec change

1. Remove 10/100 LAN (RTL8201BL).
2. Giga PHY Vitesse VSC8601SC change to Realtek RTL8211BL.

ver : 11 data : 2007 / 08 / 30

Spec change

1. SATA2 change to orange color. (N5N-07M0131-H06) .

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Title	 HISTORY FOR 0B	Rev 1.1
Document Number	MS-7295	
MICRO-STAR INT'L CO., LTD. No. 68, Li-De St, Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Thursday, August 30, 2007 Sheet 31 of 35